Sun Fire™ V1280 Service Manual

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Part No. 816-0205-10
September 2002, Revision A

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Preface

This manual describes all the procedures necessary to complete all service and maintenance on a Sun Fire V1280 system.

How This Book Is Organized

Part I: Troubleshooting

Chapter 1 describes how to isolate faults.

Part II: Preparing for Service

Chapter 2 lists the required safety procedures.

Chapter 3 describes how to power off and power on the system.

Part III: Subassembly Removal and Replacement

Chapter 4 describes how to replace individual storage devices and the entire removeable media bay.

Chapter 5 describes how to replace the various parts of the cooling system.

Chapter 6 explains how to replace the power subsystem components.

Chapter 7 describes how to remove and install CPU/Memory boards, and how to replace DIMMs.

Chapter 8 explains how to remove and install the IB_SSC assembly.

Chapter 9 explains how to remove and install the Level 2 repeater boards.

Chapter 10 describes how to replace the service indicator board.

Chapter 11 describes how to replace the baseplane.

Chapter 12 describes how to replace the antigravity c;lutch mechanism.

Part IV: Appendices

Appendix A contains details of individual field-replaceable parts.

Appendix B describes the I/O connector pinouts.

Typographic Conventions

Typeface	Meaning	Examples
`AaBbCc123`	The names of commands, files, and directories; on-screen computer output	Edit your `.login` file. Use `ls -a` to list all files. `% You have mail.`
`AaBbCc123`	What you type, when contrasted with on-screen computer output	`% su` `Password:`
AaBbCc123	Book titles, new words or terms, words to be emphasized	Read Chapter 6 in the *User's Guide.* These are called *class* options. You *must* be superuser to do this.
	Command-line variable; replace with a real name or value	To delete a file, type `rm` *filename.*

Shell Prompts

Shell	Prompt
C shell	*machine_name*%
C shell superuser	*machine_name*#
Bourne shell and Korn shell	$
Bourne shell and Korn shell superuser	#
LOM prompt	`lom>`

Related Documentation

Application	Title	Part Number
Installation	*Sun Fire V1280 Site Preparation and Installation Guide*	816-0201
System Administration	*Sun Fire V1280 System Administration Guide*	816-0204

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PART I Troubleshooting

CHAPTER 1

Fault Isolation

There are a number of different methods to obtain information about problems:

Refer also to the *Sun Fire V1280 System Administration Guide*.

1.1 Basic Troubleshooting

In a functioning Sun Fire V1280 system with no known problems, there should not be any Fault LEDs on the enclosure or any FRU. In addition, the `syslog` file and the administrative console should show no error messages. In the event of a subsequent problem or failure, the System Controller functions to attempt to determine what hardware is faulty and then take steps to prevent that hardware from being used until it has been replaced. Thus, in the event of a problem or failure, the System Controller functions as follows:

- May cause the hardware to pause while software analyzes and records the event error
- Determines whether or not the error is recoverable and if the system needs to be reset
- When possible causes the faulty FRU to provide an LED indication of a fault in addition to populating the System Console messages with further details
- Determine whether dynamic deconfiguration and reconfiguration is applicable

The following sections detail overall system functional flows in scenarios where a diagnosis cannot be made by the System Controller and further knowledge of the system functional flow is required.

This section contains the following:

1.1.1 Power Distribution

To troubleshoot the power distribution system, first ensure that all cabling is properly connected and that the positioning of switches is correct on all involved FRUs. Further, check that the LEDs on the involved FRUs are as indicated in the following sections.

1.1.1.1 Normal Operation

In a properly operating Sun Fire V1280 system, all LEDs on the FRUs should be as indicated in TABLE 1-1.

TABLE 1-1 FRU LED Status

	LED Status	
FRU	**In Standby Mode**	**After Power On**
Power supplies	Green Power LEDs blinking All other LEDs off.	Power LEDs green. All other LEDs off.
System boards	IB_SSC Power LED green. All other LEDs off.	Power LEDs green. All other LEDs off.
Main fans and fan tray	Fan tray Power LED green. All other LEDs off.	Fan tray Power LED green. All other LEDs off.
IB fans	All LEDs off.	All LEDs off.
Hard disk drives	All LEDs off.	Power LEDs green. All other LEDs off.

1.1.1.2 Abnormal Operation

Abnormal indications of faulty incoming power can be indicated by the amber fault LED being lit on one or more of the involved FRUs.

1.1.2 Fan Tray

The system has a fan tray assembly that cools all components in the system. A faulty fan tray can be identified through physical inspection or by inspecting the LEDs (see Section 1.4.2, “Interpreting LEDs” on page 1-29). Following the failure of a fan, the remaining working fans are all turned to high by the System Controller to compensate for the reduced airflow. The system is designed to operate normally under these conditions until such time as the failed fan can be serviced. The fan tray cannot be hot replaced.

1.1.3 System Controller

The System Controller contains the system clock and a System Controller. One System Controller board is required per system.

The System Controller provides:

- Programmable system and processor clock
- Serial port for the console
- Centralized Time-of-day (TOD) chip that includes NVRAM
- Centralized reset logic
- Status and control of power supplies

The System Controller consists of the following subsystems:

- Console Bus
- Clocks
- Reset logic
- Baseplane connector signals

When the SC is first powered on the firmware will test the SC components and copy the operating System and the SC application from its on-board Flash PROM storage into the SC DRAM. The SC will then start executing the SC OS which in turn will automatically start the SC application.

1.1.4 System Controller Booting (Normal Operation)

The primary responsibility for the execution and control of system POST (SPOST) lies with code executed by the System Controller CPU and CPUs located on the CPU/Memory boards. SPOST code obtained from the CPU/Memory boards’ CPU PROMs is labeled LPOST. SPOST functions executed by the System Controller, from its DRAM, are labeled SCPOST.

1.1.5 System Controller Messages

The System Controller gets error messages from each of the boards, that is, System, I/O and L2 Repeater boards. In general, error messages propagate from the L1 (located on CPU/Memory boards) and L2 Repeater boards to the System Controller. The Sun Fire BootBus Controller (SBBC) located on the SC board determines the action to take on the errors. Typical actions would be:

- Set the appropriate error status bits
- Assert Error Pause to stop further address packets
- Interrupt the SC.

At this point the SC software takes over, reading the various error status registers to find out what happened. After detecting the cause of the error the SC may decide whether the error is recoverable or not.

1.2 SunVTS

The SunVTS software executes multiple diagnostic hardware tests from a single user interface. SunVTS verifies the configuration, functionality and reliability of most hardware controllers and devices.

TABLE 1-2 lists the documentation for the SunVTS software. These documents are available on the *Solaris on Sun Hardware AnswerBook*, which is on the *Updates CD-ROM* for the Solaris release.

TABLE 1-2 SunVTS Documentation

Title	Description
SunVTS User's Guide	Describes the SunVTS environment; starting and controlling various user interfaces; feature descriptions
SunVTS Test Reference Manual	Describes each SunVTS test; provides various test options and command line arguments
SunVTS Quick Reference Card	Provides overview of `vtsui` interface features

1.3 Power On Self Test (POST)

This section contains procedures to initiate the Sun Fire V1280 system unit power-on self-test diagnostics. Procedures are also included to support pre-POST preparation, POST data interpretation and the bypassing of POST diagnostics.

The Sun Fire V1280 system is designed with an intelligent System Controller (SC) which is used for configuring, monitoring, recovering (from errors) and controlling the system. The primary responsibility for the execution and control of the various Power On Self Tests (POSTs) lies with code executed by the System Controller.

Power-on self testing consists of SCPOST (executed immediately after a power cycle or a reset of the SC and before the LOM prompt command line interface is displayed) and SPOST/LPOST (which run when the system is powered on from Standby mode). FIGURE 1-1 shows the sequence of POST tests during system power-on.

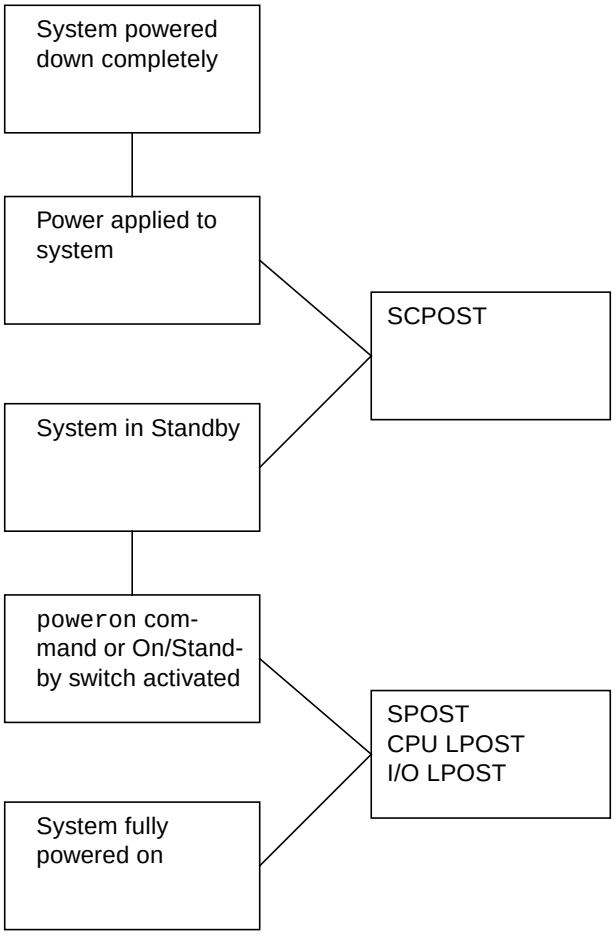


FIGURE 1-1 POST Sequence During Power-On

1.3.1 SCPOST

SCPOST is resident in the Flash PROM on the System Controller board. When entered, SCPOST will initialize and test System Controller components according to the diagnostics level specified by the LOM `setupsc` command.

1.3.2 SPOST

System POST (SPOST) is resident in the Flash PROM on the System Controller within the Java classes and methods of ScApp/LOM. It controls and sequences LPOST (CPU and I/O) and collects the results from LPOST tests.

When entered, SPOST will initialize and test System Controller components according to the diagnostics level specified by the OBP setting `diag-level`. The tests are structured such that all faults will be isolated to a failing ASIC. SPOST reports test results to the OBP and can be displayed there using the OBP `show-post-results` command.

The messages will identify the board component being tested, and provide information necessary to ascertain the operation that has failed. Some of the functions of SPOST are:

- Configuring system clocks
- System probing (using JTAG, I2C, and Console Bus)
- System interconnect tests
- System configuration
- High level system power on and sequencing of LPOST
- Maintaining the board descriptor array (hardware database)
- Gathering system error states
- Facilitating ASR

1.3.3 LPOST

LPOST (Local POST) is C code resident in each of the System Boards' Flash PROMs, that is, CPU/Memory Boards (CPU LPOST) and the I/O Board (I/O LPOST). It contains the actual diagnostics tests executed by the main system CPUs.

SPOST and LPOST communicate through SRAMs that are accessible via the Console Bus on the SC side and the Boot Bus on the Processor side.

LPOST will be entered when SPOST running on the System Controller removes Safari reset to the CPU ports. When entered, LPOST will initialize and test system CPU and I/O board components according to the diagnostic level specified by SPOST (which in normal operation is determined by the OBP setting `diag-level` but under certain circumstances, for instance during Automatic System Recovery, may be set higher). Tests are structured and executed such that faults are isolated to a failed component. Some of the functions of LPOST are:

- UltraSPARC III reset dispatching
- Configuring UltraSPARC III operating frequency
- Testing/initializing CPUs, Caches, and DIMMs
- Testing/initializing CPU/Memory board ASICs
- Testing/initializing I/O board ASICs

1.3.4 POST

POST can be used to determine if part of the system unit has failed and should be replaced. POST detects approximately 95 percent of system unit faults, and is located in the CPU/Memory board OpenBoot™ PROM (OBP). The setting of two NVRAM variables, the `diag-switch?` and `diag-level` flags, determines if POST is executed. TABLE 1-3 lists the `diag-switch?` and `diag-level` flag settings for disabling POST (`off`), enabling POST maximum (`max`), or enabling POST minimum (`min`).

The default setting for `diag-level` is `max`. An example of a `max` level POST output on serial port A is provided in Section 1.3.5.1, "`diag-level` Variable Set to `max`" on page 1-12. An example of a `min` level POST output on serial port A is provided in Section 1.3.5.2, "`diag-level` Variable Set to `min`" on page 1-24.

To set `diag-level` to `min`, type:

```
ok setenv diag-level min
```

To return to the default setting:

```
ok setenv diag-level init
```

TABLE 1-3 POST Configuration Parameters

Parameter	Value	Description
`diag-level`	`off`	POST is disabled.
	`init` (default value)	Only system board initialization code is run. No testing is done. This is a very fast pass through POST.
	`max`	All system board components are tested with all tests and test patterns, except for memory and Ecache modules. For memory and Ecache modules, all locations are tested with multiple patterns. More extensive, time-consuming algorithms are not run at this level.
	`quick`	All system board components are tested using few tests with few test patterns.
	`mem1`	Runs all tests at the default level plus more exhaustive DRAM and SRAM test algorithms.

TABLE 1-3 POST Configuration Parameters *(Continued)*

Parameter	Value	Description
	mem2	This is the same as mem1 with the addition of a DRAM test that does explicit compare operations of the DRAM data.
verbosity-level	off	No status messages are displayed.
	min (default value)	Test names status messages, and error messages are displayed.
	max	Subtest trace messages are displayed.
error-level	off	No error messages are displayed.
	min	The failing test name is displayed.
	max (default value)	All relevant error statuses are displayed.
interleave-scope	within-board (default value)	The memory banks on a CPU/Memory board will be interleaved with each other.
	across-boards	The memory will be interleaved on all memory banks across all of the CPU/Memory boards in the system.
interleave-mode	optimal (default value)	The memory is mixed-size interleaving in order to gain optimal performance.
	fixed	The memory is fixed-size interleaving.
	off	There is no memory interleaving.
reboot-on-error	false (default value)	The system will be paused when there is an error.
	true	The system will be rebooted.
use-nvramrc?		This parameter is the same as the OpenBoot PROM nvramrc? parameter. This parameter uses aliases that are stored in nvramrc.
	true	The OpenBoot PROM executes the script stored in nvramrc if this parameter is set to true.
	false (default value)	The OpenBoot PROM does not evaluate the script stored in nvramrc if this parameter is set to false.
auto-boot?		Controls booting of the Solaris operating environment.
	true (default value)	If this value is true, the system boots automatically after POST has run.
	false	If this parameter value is set to false, you will obtain the OpenBoot PROM ok prompt after POST runs, from which you must type a boot command to boot the Solaris operating environment.

TABLE 1-3 POST Configuration Parameters *(Continued)*

Parameter	Value	Description
`error-reset-recovery`		Controls the behavior of the system after an externally initiated reset (XIR) as well as a red mode trap.
	`sync` (default value)	The OpenBoot PROM invokes `sync`. A core file is generated. If the invocation returns, the OpenBoot PROM performs a reboot.
	`none`	The OpenBoot PROM prints a message describing the reset trap that triggered the error reset and passes control to the OpenBoot PROM `ok` prompt. The message describing the reset trap type is platform specific.
	`boot`	The OpenBoot PROM firmware reboots the system. A core file is not generated. Rebooting a system occurs using the OpenBoot PROM settings for `diag-device` or `boot-device`, depending on the value of the OpenBoot PROM configuration variable `diag-switch?` If `diag-switch?` is set to `true`, the device names in `diag-device` will be the default for boot. If `diag-switch?` is set to `false`, the device names in `boot-device` will be the default for boot.

Pre-POST preparation includes:

- Setting up a `tip` connection to another workstation or terminal to view POST progress and error messages. See Section 1.3.4.1, “To Set Up a `tip` Connection” on page 1-10.
- Verifying baud rates between a Sun Fire V1280 and a terminal. See Section 1.3.4.2, “To Verify the Baud Rate” on page 1-11.

1.3.4.1 To Set Up a `tip` Connection

A `tip` connection enables a remote shell window to be used as a terminal to display test data from a system being tested. Serial ports A or B are used to establish the `tip` connection between the system unit being tested and another Sun workstation monitor or TTY-type terminal. The `tip` connection is used in a SunOS window and provides features to help with the OBP.

1. **Connect serial port A of the system being tested to another Sun workstation serial port B using a serial null modem cable (connect cable pins 2-3, 3-2, 7-20, and 20-7).**
2. **At the other Sun workstation, check the `/etc/remote` file:**

```
hardwire:\
        :dv=/dev/term/b:br#9600:el=^C^S^Q^U^D:ie=%$:oe=^D:
```

Note – The example shows connection to serial port B, `ttyb`.

3. **To use serial port A:**

   a. Copy and paste the following:

```
hardwire:\
       :dv=/dev/term/b:br#9600:el=^C^S^Q^U^D:ie=%$:oe=^D:
```

   b. Then modify as follows:

```
hardwire:\
       :dv=/dev/term/a:br#9600:el=^C^S^Q^U^D:ie=%$:oe=^D:
```

4. **In a shell tool window on the Sun workstation, type `tip hardwire`. Verify the response:**

```
hostname% tip hardwire
connected
```

Note – The shell window is now a `tip` window directed to the serial port of the system unit being tested. When power is applied to the system unit being tested, POST messages will be displayed in this window.

5. **When POST is completed, disconnect the `tip` window by typing ~. (tilde+period).**

1.3.4.2 To Verify the Baud Rate

To verify the baud rate between the system unit being tested and a terminal or another Sun workstation monitor:

1. **Open a shell tool.**
2. **Type `eeprom`.**
3. **Verify the following serial port default settings as follows:**

```
ttyb-mode = 9600,8,n,1
ttya-mode = 9600,8,n,1
```

Note – Ensure that the settings are consistent with TTY-type terminal or workstation monitor settings.

1.3.4.3 To Initialize POST

POST is initialized by setting `diag-switch?` to `true` and `diag-level` to `max` or `min`, followed by powering the system down to Standby mode and then powering on again from the LOM prompt.

1. **At the system prompt, type:**

```
setenv diag-switch? true
```

2. **When the POST is complete, set `diag-switch?` to `false` (default setting).**

1.3.5 POST Output

Several levels of POST are available; refer to TABLE 1-3. Maximum (`max`) level and minimum (`min`) level are illustrated here. The system initiates the selected level of POST based on the setting of `diag-level`, an NVRAM variable.

1.3.5.1 `diag-level` Variable Set to `max`

When the `diag-level` variable is set to `max`, POST enables an extended set of diagnostic-level tests. This mode requires up to 32 minutes to complete, depending on system configuration. CODE EXAMPLE 1-1 identifies a typical serial port A POST output with `diag-level` set to `max`.

Note – xxxx placeholders used in table entries represent numeric values which can change without notice.

CODE EXAMPLE 1-1 POST Output Using `diag-level max` Setting

```
Loading the test table from board SB0 PROM 0 ...
{/N0/SB0/P0} Running CPU POR and Set Clocks
{/N0/SB0/P1} Running CPU POR and Set Clocks
{/N0/SB0/P2} Running CPU POR and Set Clocks
{/N0/SB0/P3} Running CPU POR and Set Clocks
{/N0/SB0/P0} @(#) lpost         5.12.0003       2002/03/01 08:54
{/N0/SB0/P2} @(#) lpost         5.12.0003       2002/03/01 08:54
{/N0/SB0/P1} @(#) lpost         5.12.0003       2002/03/01 08:54
{/N0/SB0/P0} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/SB0/P0} Subtest: Setting Fireplane Config Registers
{/N0/SB0/P0} Subtest: Display CPU Version, frequency
{/N0/SB0/P0} Version register = 003e0014.54000507
{/N0/SB0/P0} Cpu/System ratio = 5, cpu actual frequency = 750
{/N0/SB0/P1} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/SB0/P1} Subtest: Setting Fireplane Config Registers
{/N0/SB0/P1} Subtest: Display CPU Version, frequency
{/N0/SB0/P1} Version register = 003e0014.54000507
{/N0/SB0/P1} Cpu/System ratio = 5, cpu actual frequency = 750
{/N0/SB0/P3} @(#) lpost         5.12.0003       2002/03/01 08:54
{/N0/SB0/P2} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/SB0/P2} Subtest: Setting Fireplane Config Registers for aid 0x2
{/N0/SB0/P2} Subtest: Display CPU Version, frequency
{/N0/SB0/P2} Version register = 003e0014.54000507
{/N0/SB0/P2} Cpu/System ratio = 5, cpu actual frequency = 750
{/N0/SB0/P3} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/SB0/P3} Subtest: Setting Fireplane Config Registers for aid 0x3
{/N0/SB0/P3} Subtest: Display CPU Version, frequency
{/N0/SB0/P3} Version register = 003e0014.54000507
{/N0/SB0/P3} Cpu/System ratio = 5, cpu actual frequency = 750
{/N0/SB0/P2} Running Basic CPU
{/N0/SB0/P3} Running Basic CPU
{/N0/SB0/P2} @(#) lpost         5.12.0003       2002/03/01 08:54
{/N0/SB0/P3} @(#) lpost         5.12.0003       2002/03/01 08:54
{/N0/SB0/P2} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/SB0/P2} Subtest: I-Cache RAM Test
{/N0/SB0/P3} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/SB0/P3} Subtest: I-Cache RAM Test
{/N0/SB0/P0} Running Basic CPU
{/N0/SB0/P1} Running Basic CPU
{/N0/SB0/P0} @(#) lpost         5.12.0003       2002/03/01 08:54
{/N0/SB0/P1} @(#) lpost         5.12.0003       2002/03/01 08:54
{/N0/SB0/P0} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/SB0/P0} Subtest: I-Cache RAM Test
{/N0/SB0/P1} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/SB0/P1} Subtest: I-Cache RAM Test
```

CODE EXAMPLE 1-1 POST Output Using `diag-level max` Setting *(Continued)*

```
{/N0/SB0/P2} Subtest: I-Cache TAGS Test
{/N0/SB0/P3} Subtest: I-Cache TAGS Test
{/N0/SB0/P0} Subtest: I-Cache TAGS Test
{/N0/SB0/P1} Subtest: I-Cache TAGS Test
{/N0/SB0/P2} Subtest: I-Cache Valid/Predict TAGS Test
{/N0/SB0/P3} Subtest: I-Cache Valid/Predict TAGS Test
{/N0/SB0/P0} Subtest: I-Cache Valid/Predict TAGS Test
{/N0/SB0/P1} Subtest: I-Cache Valid/Predict TAGS Test
{/N0/SB0/P2} Subtest: I-Cache Snoop Tags Test
{/N0/SB0/P3} Subtest: I-Cache Snoop Tags Test
{/N0/SB0/P0} Subtest: I-Cache Snoop Tags Test
{/N0/SB0/P1} Subtest: I-Cache Snoop Tags Test
{/N0/SB0/P2} Subtest: I-Cache Branch Predict Array Test
{/N0/SB0/P3} Subtest: I-Cache Branch Predict Array Test
{/N0/SB0/P0} Subtest: I-Cache Branch Predict Array Test
{/N0/SB0/P1} Subtest: I-Cache Branch Predict Array Test
{/N0/SB0/P0} Subtest: I-Cache Initialization
{/N0/SB0/P1} Subtest: I-Cache Initialization
{/N0/SB0/P2} Subtest: I-Cache Initialization
{/N0/SB0/P3} Subtest: I-Cache Initialization
{/N0/SB0/P0} Subtest: D-Cache RAM Test
{/N0/SB0/P1} Subtest: D-Cache RAM Test
{/N0/SB0/P2} Subtest: D-Cache RAM Test
{/N0/SB0/P3} Subtest: D-Cache RAM Test
{/N0/SB0/P2} Subtest: D-Cache TAGS Test
{/N0/SB0/P3} Subtest: D-Cache TAGS Test
{/N0/SB0/P0} Subtest: D-Cache TAGS Test
{/N0/SB0/P1} Subtest: D-Cache TAGS Test
{/N0/SB0/P2} Subtest: D-Cache MicroTags Test
{/N0/SB0/P3} Subtest: D-Cache MicroTags Test
{/N0/SB0/P0} Subtest: D-Cache MicroTags Test
{/N0/SB0/P1} Subtest: D-Cache MicroTags Test
{/N0/SB0/P2} Subtest: D-Cache SnoopTags Test
{/N0/SB0/P3} Subtest: D-Cache SnoopTags Test
{/N0/SB0/P0} Subtest: D-Cache SnoopTags Test
{/N0/SB0/P1} Subtest: D-Cache SnoopTags Test
{/N0/SB0/P2} Subtest: D-Cache Initialization
{/N0/SB0/P3} Subtest: D-Cache Initialization
{/N0/SB0/P0} Subtest: D-Cache Initialization
{/N0/SB0/P1} Subtest: D-Cache Initialization
{/N0/SB0/P2} Subtest: W-Cache RAM Test
{/N0/SB0/P3} Subtest: W-Cache RAM Test
{/N0/SB0/P0} Subtest: W-Cache RAM Test
{/N0/SB0/P1} Subtest: W-Cache RAM Test
{/N0/SB0/P2} Subtest: W-Cache TAGS Test
{/N0/SB0/P3} Subtest: W-Cache TAGS Test
{/N0/SB0/P0} Subtest: W-Cache TAGS Test
```

CODE EXAMPLE 1-1 POST Output Using `diag-level max` Setting *(Continued)*

```
{/N0/SB0/P1} Subtest: W-Cache TAGS Test
{/N0/SB0/P2} Subtest: W-Cache Valid bit Test
{/N0/SB0/P3} Subtest: W-Cache Valid bit Test
{/N0/SB0/P0} Subtest: W-Cache Valid bit Test
{/N0/SB0/P1} Subtest: W-Cache Valid bit Test
{/N0/SB0/P2} Subtest: W-Cache Bank valid bit Test
{/N0/SB0/P3} Subtest: W-Cache Bank valid bit Test
{/N0/SB0/P0} Subtest: W-Cache Bank valid bit Test
{/N0/SB0/P1} Subtest: W-Cache Bank valid bit Test
{/N0/SB0/P2} Subtest: W-Cache SnoopTAGS Test
{/N0/SB0/P3} Subtest: W-Cache SnoopTAGS Test
{/N0/SB0/P0} Subtest: W-Cache SnoopTAGS Test
{/N0/SB0/P1} Subtest: W-Cache SnoopTAGS Test
{/N0/SB0/P2} Subtest: W-Cache Initialization
{/N0/SB0/P3} Subtest: W-Cache Initialization
{/N0/SB0/P2} Subtest: P-Cache RAM Test
{/N0/SB0/P3} Subtest: P-Cache RAM Test
{/N0/SB0/P0} Subtest: W-Cache Initialization
{/N0/SB0/P1} Subtest: W-Cache Initialization
{/N0/SB0/P0} Subtest: P-Cache RAM Test
{/N0/SB0/P1} Subtest: P-Cache RAM Test
{/N0/SB0/P2} Subtest: P-Cache TAGS Test
{/N0/SB0/P3} Subtest: P-Cache TAGS Test
{/N0/SB0/P0} Subtest: P-Cache TAGS Test
{/N0/SB0/P1} Subtest: P-Cache TAGS Test
{/N0/SB0/P2} Subtest: P-Cache SnoopTags Test
{/N0/SB0/P3} Subtest: P-Cache SnoopTags Test
{/N0/SB0/P0} Subtest: P-Cache SnoopTags Test
{/N0/SB0/P1} Subtest: P-Cache SnoopTags Test
{/N0/SB0/P2} Subtest: P-Cache Status Data Test
{/N0/SB0/P3} Subtest: P-Cache Status Data Test
{/N0/SB0/P0} Subtest: P-Cache Status Data Test
{/N0/SB0/P1} Subtest: P-Cache Status Data Test
{/N0/SB0/P2} Subtest: P-Cache Initialization
{/N0/SB0/P3} Subtest: P-Cache Initialization
{/N0/SB0/P0} Subtest: P-Cache Initialization
{/N0/SB0/P2} Subtest: Branch Prediction Initialization
{/N0/SB0/P1} Subtest: P-Cache Initialization
{/N0/SB0/P3} Subtest: Branch Prediction Initialization
{/N0/SB0/P0} Subtest: Branch Prediction Initialization
{/N0/SB0/P1} Subtest: Branch Prediction Initialization
{/N0/SB0/P2} Subtest: IMMU Registers Access
{/N0/SB0/P3} Subtest: IMMU Registers Access
{/N0/SB0/P0} Subtest: IMMU Registers Access
{/N0/SB0/P1} Subtest: IMMU Registers Access
{/N0/SB0/P2} Subtest: DMMU Registers Access
{/N0/SB0/P3} Subtest: DMMU Registers Access
```

CODE EXAMPLE 1-1 POST Output Using `diag-level max` Setting *(Continued)*

```
{/N0/SB0/P0} Subtest: DMMU Registers Access
{/N0/SB0/P1} Subtest: DMMU Registers Access
{/N0/SB0/P2} Subtest: 4M DTLB RAM Test
{/N0/SB0/P3} Subtest: 4M DTLB RAM Test
{/N0/SB0/P2} Subtest: 8K DTLB RAM Test
{/N0/SB0/P3} Subtest: 8K DTLB RAM Test
{/N0/SB0/P0} Subtest: 4M DTLB RAM Test
{/N0/SB0/P1} Subtest: 4M DTLB RAM Test
{/N0/SB0/P0} Subtest: 8K DTLB RAM Test
{/N0/SB0/P1} Subtest: 8K DTLB RAM Test
{/N0/SB0/P2} Subtest: 4M DTLB TAG Test
{/N0/SB0/P3} Subtest: 4M DTLB TAG Test
{/N0/SB0/P2} Subtest: 8K DTLB TAG Test
{/N0/SB0/P3} Subtest: 8K DTLB TAG Test
{/N0/SB0/P0} Subtest: 4M DTLB TAG Test
{/N0/SB0/P1} Subtest: 4M DTLB TAG Test
{/N0/SB0/P0} Subtest: 8K DTLB TAG Test
{/N0/SB0/P1} Subtest: 8K DTLB TAG Test
{/N0/SB0/P2} Subtest: 4M ITLB RAM Test
{/N0/SB0/P3} Subtest: 4M ITLB RAM Test
{/N0/SB0/P0} Subtest: 4M ITLB RAM Test
{/N0/SB0/P1} Subtest: 4M ITLB RAM Test
{/N0/SB0/P2} Subtest: 8K ITLB RAM Test
{/N0/SB0/P3} Subtest: 8K ITLB RAM Test
{/N0/SB0/P0} Subtest: 8K ITLB RAM Test
{/N0/SB0/P1} Subtest: 8K ITLB RAM Test
{/N0/SB0/P2} Subtest: 4M ITLB TAG Test
{/N0/SB0/P3} Subtest: 4M ITLB TAG Test
{/N0/SB0/P0} Subtest: 4M ITLB TAG Test
{/N0/SB0/P1} Subtest: 4M ITLB TAG Test
{/N0/SB0/P2} Subtest: 8K ITLB TAG Test
{/N0/SB0/P3} Subtest: 8K ITLB TAG Test
{/N0/SB0/P0} Subtest: 8K ITLB TAG Test
{/N0/SB0/P1} Subtest: 8K ITLB TAG Test
{/N0/SB0/P2} Subtest: E-Cache Global Variables Initialization
{/N0/SB0/P3} Subtest: E-Cache Global Variables Initialization
{/N0/SB0/P0} Subtest: E-Cache Global Variables Initialization
{/N0/SB0/P1} Subtest: E-Cache Global Variables Initialization
{/N0/SB0/P2} Subtest: E-Cache TAGS Test
{/N0/SB0/P3} Subtest: E-Cache TAGS Test
{/N0/SB0/P0} Subtest: E-Cache TAGS Test
{/N0/SB0/P1} Subtest: E-Cache TAGS Test
{/N0/SB0/P2} Subtest: Fast Init. Verification Test
{/N0/SB0/P3} Subtest: Fast Init. Verification Test
{/N0/SB0/P0} Subtest: Fast Init. Verification Test
{/N0/SB0/P1} Subtest: Fast Init. Verification Test
{/N0/SB0/P2} Subtest: E-Cache TAGS ECC Test
```

CODE EXAMPLE 1-1 POST Output Using `diag-level max` Setting *(Continued)*

```
{/N0/SB0/P3} Subtest: E-Cache TAGS ECC Test
{/N0/SB0/P0} Subtest: E-Cache TAGS ECC Test
{/N0/SB0/P1} Subtest: E-Cache TAGS ECC Test
{/N0/SB0/P0} Running Enable MMU
{/N0/SB0/P1} Running Enable MMU
{/N0/SB0/P0} Subtest: IMMU Initialization
{/N0/SB0/P1} Subtest: IMMU Initialization
{/N0/SB0/P2} Running Enable MMU
{/N0/SB0/P3} Running Enable MMU
{/N0/SB0/P0} Subtest: DMMU Initialization
{/N0/SB0/P1} Subtest: DMMU Initialization
{/N0/SB0/P2} Subtest: IMMU Initialization
{/N0/SB0/P3} Subtest: IMMU Initialization
{/N0/SB0/P2} Subtest: DMMU Initialization
{/N0/SB0/P3} Subtest: DMMU Initialization
{/N0/SB0/P0} Subtest: Map LPOST to local space
{/N0/SB0/P1} Subtest: Map LPOST to local space
{/N0/SB0/P2} Subtest: Map LPOST to local space
{/N0/SB0/P3} Subtest: Map LPOST to local space
{/N0/SB0/P2} Running FPU Tests
{/N0/SB0/P3} Running FPU Tests
{/N0/SB0/P2} Subtest: FPU Register Test
{/N0/SB0/P3} Subtest: FPU Register Test
{/N0/SB0/P0} Running FPU Tests
{/N0/SB0/P1} Running FPU Tests
{/N0/SB0/P0} Subtest: FPU Register Test
{/N0/SB0/P1} Subtest: FPU Register Test
{/N0/SB0/P2} Subtest: FSR Test
{/N0/SB0/P3} Subtest: FSR Test
{/N0/SB0/P0} Subtest: FSR Test
{/N0/SB0/P1} Subtest: FSR Test
{/N0/SB0/P0} Running Basic Ecache
{/N0/SB0/P1} Running Basic Ecache
{/N0/SB0/P0} Subtest: E-Cache Quick Verification Test
{/N0/SB0/P2} Running Basic Ecache
{/N0/SB0/P3} Running Basic Ecache
{/N0/SB0/P2} Subtest: E-Cache Quick Verification Test
{/N0/SB0/P1} Subtest: E-Cache Quick Verification Test
{/N0/SB0/P3} Subtest: E-Cache Quick Verification Test
{/N0/SB0/P0} Subtest: E-Cache RAM Test Part1
{/N0/SB0/P1} Subtest: E-Cache RAM Test Part1
{/N0/SB0/P2} Subtest: E-Cache RAM Test Part1
{/N0/SB0/P3} Subtest: E-Cache RAM Test Part1
{/N0/SB0/P0} Subtest: E-Cache RAM Test Part2
{/N0/SB0/P1} Subtest: E-Cache RAM Test Part2
{/N0/SB0/P2} Subtest: E-Cache RAM Test Part2
{/N0/SB0/P3} Subtest: E-Cache RAM Test Part2
```

CODE EXAMPLE 1-1 POST Output Using `diag-level max` Setting *(Continued)*

```
{/N0/SB0/P0} Subtest: E-Cache Address Line Test
{/N0/SB0/P1} Subtest: E-Cache Address Line Test
{/N0/SB0/P2} Subtest: E-Cache Address Line Test
{/N0/SB0/P3} Subtest: E-Cache Address Line Test
{/N0/SB0/P0} Subtest: E-Cache Initialization of first 1K
{/N0/SB0/P1} Subtest: E-Cache Initialization of first 1K
{/N0/SB0/P0} Subtest: E-Cache Initialization
{/N0/SB0/P1} Subtest: E-Cache Initialization
{/N0/SB0/P2} Subtest: E-Cache Initialization of first 1K
{/N0/SB0/P3} Subtest: E-Cache Initialization of first 1K
{/N0/SB0/P2} Subtest: E-Cache Initialization
{/N0/SB0/P3} Subtest: E-Cache Initialization
{/N0/SB0/P2} Running Memory Configuration Tests
{/N0/SB0/P3} Running Memory Configuration Tests
{/N0/SB0/P2} Subtest: Disable Memory Controllers
{/N0/SB0/P3} Subtest: Disable Memory Controllers
{/N0/SB0/P0} Running Memory Configuration Tests
{/N0/SB0/P1} Running Memory Configuration Tests
{/N0/SB0/P0} Subtest: Disable Memory Controllers
{/N0/SB0/P2} Subtest: Mem Addr Control Reg Test
{/N0/SB0/P1} Subtest: Disable Memory Controllers
{/N0/SB0/P3} Subtest: Mem Addr Control Reg Test
{/N0/SB0/P0} Subtest: Mem Addr Control Reg Test
{/N0/SB0/P1} Subtest: Mem Addr Control Reg Test
{/N0/SB0/P2} Subtest: Mem Addr Decoding Reg Test
{/N0/SB0/P3} Subtest: Mem Addr Decoding Reg Test
{/N0/SB0/P0} Subtest: Mem Addr Decoding Reg Test
{/N0/SB0/P1} Subtest: Mem Addr Decoding Reg Test
{/N0/SB0/P2} Subtest: Memory Controller Configuration
{/N0/SB0/P3} Subtest: Memory Controller Configuration
{/N0/SB0/P0} Subtest: Memory Controller Configuration
{/N0/SB0/P1} Subtest: Memory Controller Configuration
{/N0/SB0/P2} Subtest: UP Memory Clear
{/N0/SB0/P3} Subtest: UP Memory Clear
{/N0/SB0/P0} Subtest: UP Memory Clear
{/N0/SB0/P1} Subtest: UP Memory Clear
{/N0/SB0/P0} Running Memory Tests
{/N0/SB0/P1} Running Memory Tests
{/N0/SB0/P0} Subtest: Memory Addressing
{/N0/SB0/P2} Running Memory Tests
{/N0/SB0/P3} Running Memory Tests
{/N0/SB0/P1} Subtest: Memory Addressing
{/N0/SB0/P2} Subtest: Memory Addressing
{/N0/SB0/P3} Subtest: Memory Addressing
{/N0/SB0/P0} Subtest: Memory MATS+
{/N0/SB0/P1} Subtest: Memory MATS+
{/N0/SB0/P2} Subtest: Memory MATS+
```

CODE EXAMPLE 1-1 POST Output Using `diag-level max` Setting *(Continued)*

```
{/N0/SB0/P3} Subtest: Memory MATS+
{/N0/SB0/P2} Subtest: Memory MARCH C-
{/N0/SB0/P3} Subtest: Memory MARCH C-
{/N0/SB0/P3} Subtest: Memory Alternating Multiple Access Selection
{/N0/SB0/P2} Subtest: Memory Alternating Multiple Access Selection
{/N0/SB0/P0} Subtest: Memory MARCH C-
{/N0/SB0/P1} Subtest: Memory MARCH C-
{/N0/SB0/P0} Subtest: Memory Alternating Multiple Access Selection
{/N0/SB0/P1} Subtest: Memory Alternating Multiple Access Selection
{/N0/SB0/P0} Running Ecache Functional
{/N0/SB0/P1} Running Ecache Functional
{/N0/SB0/P0} Subtest: E-Cache Functional
{/N0/SB0/P1} Subtest: E-Cache Functional
{/N0/SB0/P2} Running Ecache Functional
{/N0/SB0/P3} Running Ecache Functional
{/N0/SB0/P2} Subtest: E-Cache Functional
{/N0/SB0/P3} Subtest: E-Cache Functional
{/N0/SB0/P2} Subtest: E-Cache Stress
{/N0/SB0/P3} Subtest: E-Cache Stress
{/N0/SB0/P0} Subtest: E-Cache Stress
{/N0/SB0/P1} Subtest: E-Cache Stress
{/N0/SB0/P2} Running CPU Functional
{/N0/SB0/P3} Running CPU Functional
{/N0/SB0/P2} Subtest: IMMU Functional
{/N0/SB0/P3} Subtest: IMMU Functional
{/N0/SB0/P2} Subtest: DMMU Functional
{/N0/SB0/P3} Subtest: DMMU Functional
{/N0/SB0/P0} Running CPU Functional
{/N0/SB0/P1} Running CPU Functional
{/N0/SB0/P0} Subtest: IMMU Functional
{/N0/SB0/P1} Subtest: IMMU Functional
{/N0/SB0/P0} Subtest: DMMU Functional
{/N0/SB0/P0} Subtest: Dual AFSR/AFAR First Error Capture Test
{/N0/SB0/P1} Subtest: DMMU Functional
{/N0/SB0/P1} Subtest: Dual AFSR/AFAR First Error Capture Test
{/N0/SB0/P1} Subtest: I-Cache Functional
{/N0/SB0/P0} Subtest: I-Cache Functional
{/N0/SB0/P2} Subtest: Dual AFSR/AFAR First Error Capture Test
{/N0/SB0/P3} Subtest: Dual AFSR/AFAR First Error Capture Test
{/N0/SB0/P2} Subtest: I-Cache Functional
{/N0/SB0/P3} Subtest: I-Cache Functional
{/N0/SB0/P2} Subtest: I-Cache Parity Functional
{/N0/SB0/P3} Subtest: I-Cache Parity Functional
{/N0/SB0/P0} Subtest: I-Cache Parity Functional
{/N0/SB0/P1} Subtest: I-Cache Parity Functional
{/N0/SB0/P2} Subtest: I-Cache Parity Tag
{/N0/SB0/P3} Subtest: I-Cache Parity Tag
```

CODE EXAMPLE 1-1 POST Output Using `diag-level max` Setting *(Continued)*

```
{/N0/SB0/P0} Subtest: I-Cache Parity Tag
{/N0/SB0/P2} Subtest: I-Cache Snoop Parity Tag
{/N0/SB0/P1} Subtest: I-Cache Parity Tag
{/N0/SB0/P3} Subtest: I-Cache Snoop Parity Tag
{/N0/SB0/P0} Subtest: I-Cache Snoop Parity Tag
{/N0/SB0/P1} Subtest: I-Cache Snoop Parity Tag
{/N0/SB0/P2} Subtest: D-Cache Functional
{/N0/SB0/P3} Subtest: D-Cache Functional
{/N0/SB0/P0} Subtest: D-Cache Functional
{/N0/SB0/P1} Subtest: D-Cache Functional
{/N0/SB0/P2} Subtest: D-Cache Parity Functional
{/N0/SB0/P3} Subtest: D-Cache Parity Functional
{/N0/SB0/P0} Subtest: D-Cache Parity Functional
{/N0/SB0/P1} Subtest: D-Cache Parity Functional
{/N0/SB0/P2} Subtest: D-Cache Parity Tag Test
{/N0/SB0/P3} Subtest: D-Cache Parity Tag Test
{/N0/SB0/P0} Subtest: D-Cache Parity Tag Test
{/N0/SB0/P1} Subtest: D-Cache Parity Tag Test
{/N0/SB0/P2} Subtest: W-Cache Functional
{/N0/SB0/P3} Subtest: W-Cache Functional
{/N0/SB0/P0} Subtest: W-Cache Functional
{/N0/SB0/P1} Subtest: W-Cache Functional
{/N0/SB0/P2} Subtest: P-Cache Functional
{/N0/SB0/P3} Subtest: P-Cache Functional
{/N0/SB0/P0} Subtest: P-Cache Functional
{/N0/SB0/P1} Subtest: P-Cache Functional
{/N0/SB0/P2} Subtest: FPU Functional
{/N0/SB0/P3} Subtest: FPU Functional
{/N0/SB0/P0} Subtest: FPU Functional
{/N0/SB0/P1} Subtest: FPU Functional
{/N0/SB0/P2} Subtest: Graphics Functional
{/N0/SB0/P3} Subtest: Graphics Functional
{/N0/SB0/P0} Subtest: Graphics Functional
{/N0/SB0/P1} Subtest: Graphics Functional
{/N0/SB0/P0} Running Advanced CPU Tests
{/N0/SB0/P1} Running Advanced CPU Tests
{/N0/SB0/P0} Subtest: CPU Superscalar Dispatch
{/N0/SB0/P1} Subtest: CPU Superscalar Dispatch
{/N0/SB0/P2} Running Advanced CPU Tests
{/N0/SB0/P3} Running Advanced CPU Tests
{/N0/SB0/P2} Subtest: CPU Superscalar Dispatch
{/N0/SB0/P3} Subtest: CPU Superscalar Dispatch
{/N0/SB0/P0} Subtest: SPARC Atomic Instruction Test
{/N0/SB0/P1} Subtest: SPARC Atomic Instruction Test
{/N0/SB0/P2} Subtest: SPARC Atomic Instruction Test
{/N0/SB0/P3} Subtest: SPARC Atomic Instruction Test
{/N0/SB0/P0} Subtest: Non SPARC Atomic Instruction Test
```

CODE EXAMPLE 1-1 POST Output Using `diag-level max` Setting *(Continued)*

```
{/N0/SB0/P1} Subtest: Non SPARC Atomic Instruction Test
{/N0/SB0/P2} Subtest: Non SPARC Atomic Instruction Test
{/N0/SB0/P3} Subtest: Non SPARC Atomic Instruction Test
{/N0/SB0/P0} Subtest: SOFTINT Register and Interrupt Test
{/N0/SB0/P1} Subtest: SOFTINT Register and Interrupt Test
{/N0/SB0/P2} Subtest: SOFTINT Register and Interrupt Test
{/N0/SB0/P3} Subtest: SOFTINT Register and Interrupt Test
{/N0/SB0/P0} Subtest: CPU Tick and Tick Compare Registers Test
{/N0/SB0/P1} Subtest: CPU Tick and Tick Compare Registers Test
{/N0/SB0/P2} Subtest: CPU Tick and Tick Compare Registers Test
{/N0/SB0/P3} Subtest: CPU Tick and Tick Compare Registers Test
{/N0/SB0/P0} Subtest: CPU Stick and Stick Compare Registers Test
{/N0/SB0/P1} Subtest: CPU Stick and Stick Compare Registers Test
{/N0/SB0/P2} Subtest: CPU Stick and Stick Compare Registers Test
{/N0/SB0/P3} Subtest: CPU Stick and Stick Compare Registers Test
{/N0/SB0/P0} Subtest: FPU Move to Registers Test
{/N0/SB0/P1} Subtest: FPU Move to Registers Test
{/N0/SB0/P2} Subtest: FPU Move to Registers Test
{/N0/SB0/P3} Subtest: FPU Move to Registers Test
{/N0/SB0/P0} Subtest: FPU Branch Test
{/N0/SB0/P1} Subtest: FPU Branch Test
{/N0/SB0/P2} Subtest: FPU Branch Test
{/N0/SB0/P3} Subtest: FPU Branch Test
{/N0/SB0/P0} Subtest: Branch Memory Test
{/N0/SB0/P1} Subtest: Branch Memory Test
{/N0/SB0/P2} Subtest: Branch Memory Test
{/N0/SB0/P3} Subtest: Branch Memory Test
{/N0/SB0/P2} Running CPU ECC Tests
{/N0/SB0/P3} Running CPU ECC Tests
{/N0/SB0/P0} Running CPU ECC Tests
{/N0/SB0/P1} Running CPU ECC Tests
{/N0/SB0/P0} Subtest: Fast ECC errors test
{/N0/SB0/P1} Subtest: Fast ECC errors test
{/N0/SB0/P2} Subtest: Fast ECC errors test
{/N0/SB0/P3} Subtest: Fast ECC errors test
{/N0/SB0/P2} Subtest: MTAG ECC errors test
{/N0/SB0/P3} Subtest: MTAG ECC errors test
{/N0/SB0/P0} Subtest: MTAG ECC errors test
{/N0/SB0/P1} Subtest: MTAG ECC errors test
{/N0/SB0/P2} Subtest: SYSTEM ECC errors test
{/N0/SB0/P3} Subtest: SYSTEM ECC errors test
{/N0/SB0/P0} Subtest: SYSTEM ECC errors test
{/N0/SB0/P1} Subtest: SYSTEM ECC errors test
{/N0/SB0/P2} Subtest: Ecache Tag ECC errors test
{/N0/SB0/P3} Subtest: Ecache Tag ECC errors test
{/N0/SB0/P0} Subtest: Ecache Tag ECC errors test
{/N0/SB0/P1} Subtest: Ecache Tag ECC errors test
```

CODE EXAMPLE 1-1 POST Output Using `diag-level max` Setting *(Continued)*

```
{/N0/SB0/P0} Running System Level Tests
{/N0/SB0/P1} Running System Level Tests
{/N0/SB0/P0} Subtest: MP Memory Access Test
{/N0/SB0/P1} Subtest: MP Memory Access Test
{/N0/SB0/P2} Running System Level Tests
{/N0/SB0/P3} Running System Level Tests
{/N0/SB0/P2} Subtest: MP Memory Access Test
{/N0/SB0/P3} Subtest: MP Memory Access Test
{/N0/SB0/P0} Running Board Memory Interleave
{/N0/SB0/P1} Running Board Memory Interleave
{/N0/SB0/P0} Subtest: Board Memory Interleave Configuration
{/N0/SB0/P1} Subtest: Board Memory Interleave Configuration
{/N0/SB0/P2} Running Board Memory Interleave
{/N0/SB0/P3} Running Board Memory Interleave
{/N0/SB0/P2} Subtest: Board Memory Interleave Configuration
{/N0/SB0/P3} Subtest: Board Memory Interleave Configuration
{/N0/SB0/P0} Passed
{/N0/SB0/P1} Passed
{/N0/SB0/P2} Passed
{/N0/SB0/P3} Passed
Testing IO Boards ...
Loading the test table from board IB6 PROM 0 ...
Copying IO prom to Cpu dram ....................................
{/N0/SB0/P0} Running PCI IO Controller Basic Tests
{/N0/SB0/P0} Jumping to memory 00000000.00000020 [00000010]
{/N0/SB0/P0} System PCI IO post code running from memory
{/N0/SB0/P0} @(#) lpost         5.12.0003       2002/03/01 09:00
{/N0/SB0/P0} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/SB0/P0} Subtest: PCI IO Controller Register Initialization for aid 0x18
{/N0/SB0/P0} Running PCI IO Controller Functional Tests
{/N0/SB0/P0} Subtest: PCI IO Controller IOMMU  TLB Compare Tests for aid 0x18
{/N0/SB0/P0} Subtest: PCI IO Controller IOMMU TLB Flush Tests for aid 0x18
{/N0/SB0/P0} Subtest: PCI IO Controller DMA loopback Tests for aid 0x18
{/N0/SB0/P0} Subtest: PCI IO Controller block DMA loopback Tests for aid 0x18
{/N0/SB0/P0} Subtest: PCI IO Controller Interrupt Tests for aid 0x18
{/N0/SB0/P0} Subtest: PCI IO Controller MergeBuffer Tests for aid 0x18
{/N0/SB0/P0} Subtest: PCI IO Controller StreamCache Tests for aid 0x18
{/N0/SB0/P0} Running PCI IO Controller Ecc Tests
{/N0/SB0/P0} Subtest: PCI IO Controller ECC Tests for aid 0x18
{/N0/SB0/P0} Running SBBC Basic Tests
{/N0/SB0/P0} Subtest: SBBC PCI Reg Initialization for aid 0x18
{/N0/SB0/P0} Running IDE Controller Tests
{/N0/SB0/P0} Subtest: IDE Controller PCI Config Space Test for aid 0x18
{/N0/SB0/P0} Running SCSI Controller Tests
{/N0/SB0/P0} Subtest: SCSI Controller PCI Config Space Test for aid 0x18
{/N0/SB0/P0} Running PCI IO Controller Basic Tests
{/N0/SB0/P0} Subtest: PCI IO Controller Register Initialization for aid 0x19
```

CODE EXAMPLE 1-1 POST Output Using `diag-level max` Setting *(Continued)*

```
{/N0/SB0/P0} Running PCI IO Controller Functional Tests
{/N0/SB0/P0} Subtest: PCI IO Controller IOMMU  TLB Compare Tests for aid 0x19
{/N0/SB0/P0} Subtest: PCI IO Controller IOMMU TLB Flush Tests for aid 0x19
{/N0/SB0/P0} Subtest: PCI IO Controller DMA loopback Tests for aid 0x19
{/N0/SB0/P0} Subtest: PCI IO Controller block DMA loopback Tests for aid 0x19
{/N0/SB0/P0} Subtest: PCI IO Controller Interrupt Tests for aid 0x19
{/N0/SB0/P0} Subtest: PCI IO Controller MergeBuffer Tests for aid 0x19
{/N0/SB0/P0} Subtest: PCI IO Controller StreamCache Tests for aid 0x19
{/N0/SB0/P0} Running PCI IO Controller Ecc Tests
{/N0/SB0/P0} Subtest: PCI IO Controller ECC Tests for aid 0x19
{/N0/SB0/P0} Running Ethernet0 Tests
{/N0/SB0/P0} Subtest: Ethernet0 PCI Config Space Test for aid 0x19
{/N0/SB0/P0} Running Ethernet1 Tests
{/N0/SB0/P0} Subtest: Ethernet1 PCI Config Space Test for aid 0x19
{/N0/SB0/P0} @(#) lpost         5.12.0003       2002/03/01 08:54
{/N0/SB0/P0} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/IB6/P0} Passed
{/N0/IB6/P1} Passed
Testing domain ...
{/N0/SB0/P0} Running Domain Level Tests
{/N0/SB0/P0} GLOBAL IO SRAM on board 6
{/N0/SB0/P0} Subtest: Mapping IO SRAM
{/N0/SB0/P0} GLOBAL IO SRAM on board 6
{/N0/SB0/P0} Subtest: Memory interleaving config
{/N0/SB0/P0} Running Domain Basic Tests
{/N0/SB0/P0} Subtest: Cross Call Test
{/N0/SB0/P0} Running Domain Advanced Tests
{/N0/SB0/P0} Subtest: MP Memory Clear Test
{/N0/SB0/P0}  CPU 1 clearing 00000000.00000000 to 00000000.80000000
{/N0/SB0/P0}  CPU 2 clearing 00000000.80000000 to 00000001.00000000
{/N0/SB0/P0}  CPU 3 clearing 00000001.00000000 to 00000001.80000000
{/N0/SB0/P0}  CPU 0 clearing 00000001.80000000 to 00000002.00000000
{/N0/SB0/P0} Subtest: DCache Snoop Tag Parity Test
{/N0/SB0/P0} Subtest: MP Cache Coherency Test
{/N0/SB0/P0} Subtest: Memory Controller Saturation Test
{/N0/SB0/P0}    All CPUs saturate /SB0/P0's memory controller
{/N0/SB0/P0}    All CPUs saturate /SB0/P1's memory controller
{/N0/SB0/P0}    All CPUs saturate /SB0/P2's memory controller
{/N0/SB0/P0}    All CPUs saturate /SB0/P3's memory controller
{/N0/SB0/P0}    All CPUs saturate /SB0/P0's memory controller
{/N0/SB0/P0}    All CPUs saturate /SB0/P1's memory controller
{/N0/SB0/P0}    All CPUs saturate /SB0/P2's memory controller
{/N0/SB0/P0}    All CPUs saturate /SB0/P3's memory controller
{/N0/SB0/P0} Subtest: Fireplane Bus Saturation Test
{/N0/SB0/P0} Subtest: MP Memory Clear Test
{/N0/SB0/P0}  CPU 1 clearing 00000000.00000000 to 00000000.80000000
{/N0/SB0/P0}  CPU 2 clearing 00000000.80000000 to 00000001.00000000
```

CODE EXAMPLE 1-1 POST Output Using `diag-level max` Setting *(Continued)*

```
{/N0/SB0/P0}  CPU 3 clearing 00000001.00000000 to 00000001.80000000
{/N0/SB0/P0}  CPU 0 clearing 00000001.80000000 to 00000002.00000000
{/N0/SB0/P0} Running Domain Stick Sync Tests
{/N0/SB0/P0} Subtest: Sync. Stick Registers Test
{/N0/SB0/P0} Running Domain Verify Stick Sync Tests
{/N0/SB0/P0} Subtest: Verify Sync. Stick Registers Test
{/N0/SB0/P0} DCB_DECOMP_OBP command succeeded
{/N0/SB0/P0} GLOBAL IO SRAM on board 6
{/N0/SB0/P0} Decompress OBP done
{/N0/SB0/P0} DCB_ENTER_OBP command succeeded
{/N0/SB0/P1} DCB_ENTER_OBP command succeeded
{/N0/SB0/P2} DCB_ENTER_OBP command succeeded
{/N0/SB0/P3} DCB_ENTER_OBP command succeeded
Entering OBP ...

Apr 10 16:26:02 some_name lom: Manufacture Date unknown - using current date
pci bootbus-controller pci
Probing /ssm@0,0/pci@18,700000 Device 1  Nothing there
Probing /ssm@0,0/pci@18,700000 Device 2  Nothing there
Probing /ssm@0,0/pci@18,700000 Device 3  ide disk cdrom
Probing /ssm@0,0/pci@18,600000 Device 1  Nothing there
Probing /ssm@0,0/pci@18,600000 Device 2  scsi disk tape scsi disk tape
pci pci
Probing /ssm@0,0/pci@19,700000 Device 1  Nothing there
Probing /ssm@0,0/pci@19,700000 Device 2  Nothing there
Probing /ssm@0,0/pci@19,700000 Device 3  Nothing there
Probing /ssm@0,0/pci@19,600000 Device 1  network
Probing /ssm@0,0/pci@19,600000 Device 2  network

Sun Fire V1280
OpenFirmware version 5.12.0003 (03/01/02 08:54)
Copyright 2001 Sun Microsystems, Inc.  All rights reserved.
SmartFirmware, Copyright (C) 1996-2001.  All rights reserved.
8192 MB memory installed, Serial #9537054.
Ethernet address 8:0:xx:xx:xx:xx, Host ID: 80xxxxxx.


NOTICE: obp_main: Extended diagnostics are now switched on.
{0} ok
```

1.3.5.2 `diag-level` Variable Set to `min`

When `diag-level` is set to `min`, POST enables an abbreviated set of diagnostic-level tests. This mode requires up to eight minutes to complete, depending on system configuration. CODE EXAMPLE 3-2 identifies a serial port A POST output with `diag-level` set to `min`.

CODE EXAMPLE 1-2 POST Output Using `diag-level min` Setting

```
.{/N0/SB0/P0} @(#) lpost        5.13.0006       2002/06/18 15:28
{/N0/SB0/P0} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
.....................................{/N0/SB0/P0} Running PCI IO Controller
Bas
ic Tests
{/N0/SB0/P0} Jumping to memory 00000000.00000020 [00000010]
{/N0/SB0/P0} System PCI IO post code running from memory
{/N0/SB0/P0} @(#) lpost         5.13.0005       2002/05/17 11:15
{/N0/SB0/P0} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/SB0/P0} Subtest: PCI IO Controller Register Initialization for aid 0x18
{/N0/SB0/P0} Running PCI IO Controller Functional Tests
{/N0/SB0/P0} Running SBBC Basic Tests
{/N0/SB0/P0} Subtest: SBBC PCI Reg Initialization for aid 0x18
{/N0/SB0/P0} Running IDE Controller Tests
{/N0/SB0/P0} Subtest: IDE Controller PCI Config Space Test for aid 0x18
{/N0/SB0/P0} Running SCSI Controller Tests
{/N0/SB0/P0} Subtest: SCSI Controller PCI Config Space Test for aid 0x18
{/N0/SB0/P0} Running PCI IO Controller Basic Tests
{/N0/SB0/P0} Subtest: PCI IO Controller Register Initialization for aid 0x19
{/N0/SB0/P0} Running PCI IO Controller Functional Tests
{/N0/SB0/P0} Running Ethernet0 Tests
{/N0/SB0/P0} Subtest: Ethernet0 PCI Config Space Test for aid 0x19
{/N0/SB0/P0} Running Ethernet1 Tests
{/N0/SB0/P0} Subtest: Ethernet1 PCI Config Space Test for aid 0x19
{/N0/SB0/P0} @(#) lpost         5.13.0006       2002/06/18 15:28
{/N0/SB0/P0} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/SB0/P1} @(#) lpost         5.13.0006       2002/06/18 15:28
{/N0/SB0/P1} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/IB6/P0} Passed
{/N0/IB6/P1} Passed
{/N0/SB0/P0} Running Domain Level Tests
{/N0/SB0/P2} @(#) lpost         5.13.0006       2002/06/18 15:28
{/N0/SB0/P3} @(#) lpost         5.13.0006       2002/06/18 15:28
{/N0/SB2/P0} @(#) lpost         5.13.0006       2002/06/18 15:28
{/N0/SB2/P1} @(#) lpost         5.13.0006       2002/06/18 15:28
{/N0/SB2/P2} @(#) lpost         5.13.0006       2002/06/18 15:28
{/N0/SB2/P3} @(#) lpost         5.13.0006       2002/06/18 15:28
{/N0/SB4/P0} @(#) lpost         5.13.0006       2002/06/18 15:28
{/N0/SB4/P1} @(#) lpost         5.13.0006       2002/06/18 15:28
{/N0/SB4/P2} @(#) lpost         5.13.0006       2002/06/18 15:28
{/N0/SB4/P3} @(#) lpost         5.13.0006       2002/06/18 15:28
{/N0/SB0/P2} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/SB0/P3} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/SB2/P0} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/SB2/P1} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
```

CODE EXAMPLE 1-2 POST Output Using `diag-level min` Setting *(Continued)*

```
{/N0/SB2/P2} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/SB2/P3} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/SB4/P0} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/SB4/P1} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/SB4/P2} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/SB4/P3} Copyright 2001 Sun Microsystems, Inc. All rights reserved.
{/N0/SB0/P0} Running Domain Basic Tests
{/N0/SB0/P0} Running Domain Advanced Tests
{/N0/SB0/P0} Running Domain Stick Sync Tests
{/N0/SB0/P0} Running Domain Verify Stick Sync Tests
{/N0/SB0/P0} DCB_DECOMP_OBP command succeeded
{/N0/SB0/P0} Committing retained memory 00000000.00b66000-00000000.00b67fff
{/N0/SB0/P0} Retaining 00000000.00b66000-00000000.00b67fff
{/N0/SB0/P0} Committing retained memory 00000000.00b88000-00000000.00b89fff
{/N0/SB0/P0} Retaining 00000000.00b88000-00000000.00b89fff
{/N0/SB0/P0}  CPU 1 clearing 00000000.00000000 to 00000000.000f3280
{/N0/SB0/P0}  CPU 2 clearing 00000000.000f3280 to 00000000.001e6500
{/N0/SB0/P0}  CPU 3 clearing 00000000.001e6500 to 00000000.002d9780
{/N0/SB0/P0}  CPU 8 clearing 00000000.002d9780 to 00000000.003cca00
{/N0/SB0/P0}  CPU 9 clearing 00000000.003cca00 to 00000000.004bfc80
{/N0/SB0/P0}  CPU 10 clearing 00000000.004bfc80 to 00000000.005b2f00
{/N0/SB0/P0}  CPU 11 clearing 00000000.005b2f00 to 00000000.006a6180
{/N0/SB0/P0}  CPU 16 clearing 00000000.006a6180 to 00000000.00799400
{/N0/SB0/P0}  CPU 17 clearing 00000000.00799400 to 00000000.0088c680
{/N0/SB0/P0}  CPU 18 clearing 00000000.0088c680 to 00000000.0097f900
{/N0/SB0/P0}  CPU 19 clearing 00000000.0097f900 to 00000000.00a72b80
{/N0/SB0/P0}  CPU 0 clearing 00000000.00a72b80 to 00000000.00b66000
{/N0/SB0/P0}  CPU 1 clearing 00000000.00b68000 to 00000000.00b6aa80
{/N0/SB0/P0}  CPU 2 clearing 00000000.00b6aa80 to 00000000.00b6d500
{/N0/SB0/P0}  CPU 3 clearing 00000000.00b6d500 to 00000000.00b6ff80
{/N0/SB0/P0}  CPU 8 clearing 00000000.00b6ff80 to 00000000.00b72a00
{/N0/SB0/P0}  CPU 9 clearing 00000000.00b72a00 to 00000000.00b75480
{/N0/SB0/P0}  CPU 10 clearing 00000000.00b75480 to 00000000.00b77f00
{/N0/SB0/P0}  CPU 11 clearing 00000000.00b77f00 to 00000000.00b7a980
{/N0/SB0/P0}  CPU 16 clearing 00000000.00b7a980 to 00000000.00b7d400
{/N0/SB0/P0}  CPU 17 clearing 00000000.00b7d400 to 00000000.00b7fe80
{/N0/SB0/P0}  CPU 18 clearing 00000000.00b7fe80 to 00000000.00b82900
{/N0/SB0/P0}  CPU 19 clearing 00000000.00b82900 to 00000000.00b85380
{/N0/SB0/P0}  CPU 0 clearing 00000000.00b85380 to 00000000.00b88000
{/N0/SB0/P0}  CPU 1 clearing 00000000.00b8a000 to 00000000.55fe9280
{/N0/SB0/P0}  CPU 2 clearing 00000000.55fe9280 to 00000000.ab448500
{/N0/SB0/P0}  CPU 3 clearing 00000000.ab448500 to 00000001.008a7780
{/N0/SB0/P0}  CPU 8 clearing 00000001.008a7780 to 00000001.55d06a00
{/N0/SB0/P0}  CPU 9 clearing 00000001.55d06a00 to 00000001.ab165c80
{/N0/SB0/P0}  CPU 10 clearing 00000001.ab165c80 to 00000002.005c4f00
{/N0/SB0/P0}  CPU 11 clearing 00000002.005c4f00 to 00000002.55a24180
{/N0/SB0/P0}  CPU 16 clearing 00000002.55a24180 to 00000002.aae83400
```

CODE EXAMPLE 1-2 POST Output Using `diag-level min` Setting *(Continued)*

```
{/N0/SB0/P0}  CPU 17 clearing 00000002.aae83400 to 00000003.002e2680
{/N0/SB0/P0}  CPU 18 clearing 00000003.002e2680 to 00000003.55741900
{/N0/SB0/P0}  CPU 19 clearing 00000003.55741900 to 00000003.aaba0b80
{/N0/SB0/P0}  CPU 0 clearing 00000003.aaba0b80 to 00000004.00000000
{/N0/SB0/P0}  CPU 1 clearing 00000020.00000000 to 00000020.55555540
{/N0/SB0/P0}  CPU 2 clearing 00000020.55555540 to 00000020.aaaaaa80
{/N0/SB0/P0}  CPU 3 clearing 00000020.aaaaaa80 to 00000020.ffffffc0
{/N0/SB0/P0}  CPU 8 clearing 00000020.ffffffc0 to 00000021.55555500
{/N0/SB0/P0}  CPU 9 clearing 00000021.55555500 to 00000021.aaaaaa40
{/N0/SB0/P0}  CPU 10 clearing 00000021.aaaaaa40 to 00000021.ffffff80
{/N0/SB0/P0}  CPU 11 clearing 00000021.ffffff80 to 00000022.555554c0
{/N0/SB0/P0}  CPU 16 clearing 00000022.555554c0 to 00000022.aaaaaa00
{/N0/SB0/P0}  CPU 17 clearing 00000022.aaaaaa00 to 00000022.ffffff40
{/N0/SB0/P0}  CPU 18 clearing 00000022.ffffff40 to 00000023.55555480
{/N0/SB0/P0}  CPU 19 clearing 00000023.55555480 to 00000023.aaaaa9c0
{/N0/SB0/P0}  CPU 0 clearing 00000023.aaaaa9c0 to 00000024.00000000
{/N0/SB0/P0}  CPU 1 clearing 00000040.00000000 to 00000040.55555540
{/N0/SB0/P0}  CPU 2 clearing 00000040.55555540 to 00000040.aaaaaa80
{/N0/SB0/P0}  CPU 3 clearing 00000040.aaaaaa80 to 00000040.ffffffc0
{/N0/SB0/P0}  CPU 8 clearing 00000040.ffffffc0 to 00000041.55555500
{/N0/SB0/P0}  CPU 9 clearing 00000041.55555500 to 00000041.aaaaaa40
{/N0/SB0/P0}  CPU 10 clearing 00000041.aaaaaa40 to 00000041.ffffff80
{/N0/SB0/P0}  CPU 11 clearing 00000041.ffffff80 to 00000042.555554c0
{/N0/SB0/P0}  CPU 16 clearing 00000042.555554c0 to 00000042.aaaaaa00
{/N0/SB0/P0}  CPU 17 clearing 00000042.aaaaaa00 to 00000042.ffffff40
{/N0/SB0/P0}  CPU 18 clearing 00000042.ffffff40 to 00000043.55555480
{/N0/SB0/P0}  CPU 19 clearing 00000043.55555480 to 00000043.aaaaa9c0
{/N0/SB0/P0}  CPU 0 clearing 00000043.aaaaa9c0 to 00000044.00000000
{/N0/SB0/P0} Decompress OBP done
{/N0/SB0/P0} DCB_ENTER_OBP command succeeded
{/N0/SB0/P1} DCB_ENTER_OBP command succeeded
{/N0/SB0/P2} DCB_ENTER_OBP command succeeded
{/N0/SB0/P3} DCB_ENTER_OBP command succeeded
{/N0/SB2/P0} DCB_ENTER_OBP command succeeded
{/N0/SB2/P1} DCB_ENTER_OBP command succeeded
{/N0/SB2/P2} DCB_ENTER_OBP command succeeded
{/N0/SB2/P3} DCB_ENTER_OBP command succeeded
{/N0/SB4/P0} DCB_ENTER_OBP command succeeded
{/N0/SB4/P1} DCB_ENTER_OBP command succeeded
{/N0/SB4/P2} DCB_ENTER_OBP command succeeded
{/N0/SB4/P3} DCB_ENTER_OBP command succeeded

pci bootbus-controller pci
Probing /ssm@0,0/pci@18,700000 Device 1  SUNW,ma
Probing /ssm@0,0/pci@18,700000 Device 2  Nothing there
Probing /ssm@0,0/pci@18,700000 Device 3  ide disk cdrom
Probing /ssm@0,0/pci@18,600000 Device 1  Nothing there
```

CODE EXAMPLE 1-2 POST Output Using `diag-level min` Setting *(Continued)*

```
Probing /ssm@0,0/pci@18,600000 Device 2  scsi disk tape scsi disk tape
pci pci
Probing /ssm@0,0/pci@19,700000 Device 1  Nothing there
Probing /ssm@0,0/pci@19,700000 Device 2  pci1214,334
Probing /ssm@0,0/pci@19,700000 Device 3  Nothing there
Probing /ssm@0,0/pci@19,600000 Device 1  network
Probing /ssm@0,0/pci@19,600000 Device 2  network

Sun Fire V1280
OpenFirmware version 5.13.0006 (06/18/02 15:28)
Copyright 2001 Sun Microsystems, Inc.  All rights reserved.
SmartFirmware, Copyright (C) 1996-2001.  All rights reserved.
49152 MB memory installed, Serial #9537018.
Ethernet address 8:0:20:91:85:fa, Host ID: 809185fa.
```

1.4 Other Fault Isolation Aids

There are a number of system fault isolation aids in addition to SunVTS™ and POST. As well as the System Controller, there are system and individual board and assembly LEDs, Sun Management Center, and OpenBoot™. Each of these items is discussed in the sections that follow:

1.4.1 System Controller

The primary responsibility for the collection, interpretation and subsequent system responsive actions regarding error messages lies with the System Controller (SC). The System Controller receives error messages from each of the boards, that is, CPU/Memory boards, I/O board and Fireplane switches.

The BootBus Controller (SBBC) located on the SC board determines the action to take on the errors. Typical actions would be:

- Set the appropriate error status bits

- Assert Error Pause to stop further address packets
- Interrupt the SC.

At this point the SC software takes over, reading the various error status registers to find out what happened. After detecting the cause of the error the SC may decide whether the error is recoverable or not.

If the error is recoverable, the SC can clear the error status in the appropriate registers in the boards that detected the error. If the error is not recoverable, the SC may decide to reset the system.

1.4.1.1 System Controller CLI

The System Controller command line interface has two levels of use:

- User (default)
- Service

1.4.1.2 ECC and Parity Errors

The DRAM, data interconnects, DCDS (dual CPU data switch), and DX chips are covered by both parity and ECC (error checking and correction codes). The entire data path from the Ultra SPARC-III data pins, through the data buffers, local data switch and the memory subsystem is protected with ECC.

While ECC provides end-to-end data protection, parity is used throughout the system on all interconnects to allow specific detection of any interconnect errors. Parity is regenerated at all interconnects to provide simple and precise fault isolation.

In general, error messages propagate from the L1 Address Repeaters and L2 Repeaters to the System Controller. The BootBus Controller (SBBC) located on the SC determines the action to take on the errors.

1.4.2 Interpreting LEDs

Use the LEDs on the individual system components to determine if the system is operating normally. That is, the LEDs should be routinely monitored on:

- Boards (System Controller and I/O Assembly (IB_SSC), CPU/Memory, L2 Repeaters)
- Fan trays
- Power supplies

LEDs can be off or on. When the fault LED is on (lit), this indicates that a fault has occurred in the system. When the fault LED is lit, you should take immediate action to clear the fault.

Note – The green Power LED on a power supply will blink when the system is in Standby mode.

You can only remove a hot-swappable powered-up component when the amber Removal OK LED is lit. TABLE 1-5 lists the LED status codes for the system and for the following hot-swappable components:

- CPU / Memory boards
- Power supplies
- Fans (main and IB)
- Hard disk drives

Note – The Fan tray, IB_SSC, and L2 Repeaters are not hot-swappable. You must power off the system in order to remove them.

Note – The main fans do not have OK to Remove LEDs.

System (Enclosure-Level) LEDs

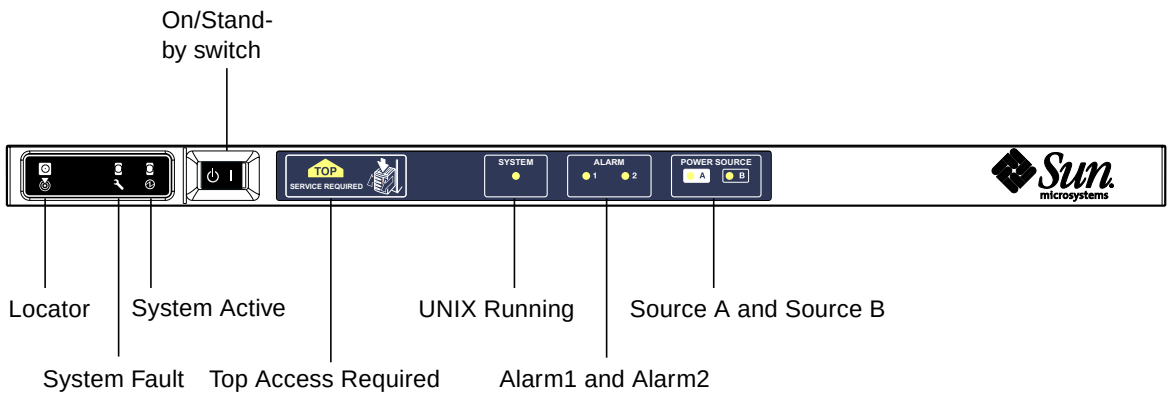


FIGURE 1-2 System Indicator Board

The enclosure-level indicator LEDs function as shown in TABLE 1-4.

TABLE 1-4 System (Enclosure-Level) Indicator LED Functions

Name	Colour	Function
Locator	White	Normally off; can be lit by user command.
System Fault	Amber	Lights when the LOM detects a fault.
System Active	Green	Lights when power is applied to the system (that is, when the system is being powered on, or is powered on). Extinguished when the system is in Standby.
Top Access	Amber	Lights when a fault occurs in a FRU which can only be replaced from the top of the system.
UNIX Running	Green	Extinguished when a fault is detected and the system is not running correctly.
Alarm1 and Alarm2	Green	Light when triggered by events as specified in the LOM.
Source A and Source B	Green	Light when the relevant power feeds are present in Standby mode.

The Locator, System Fault and System Active LEDs are repeated on the rear of the system, as shown in FIGURE 1-3.

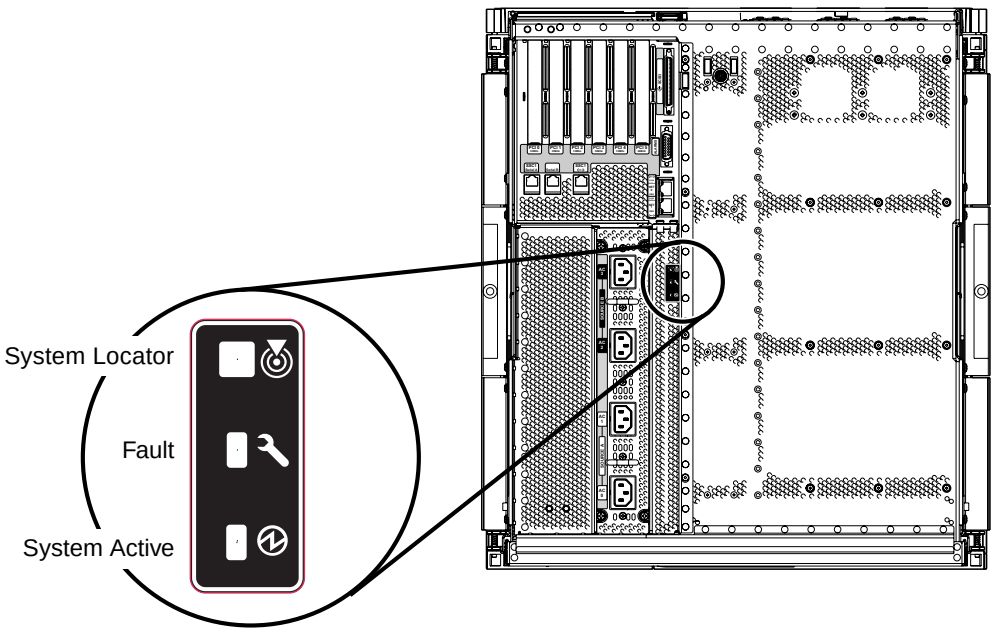


FIGURE 1-3 Enclosure Level System Indicator LED Repeater on the Back Panel

Module/Component-Level LEDs

The locations of the module and component indicator LEDs are shown in FIGURE 1-4 to FIGURE 1-9.

TABLE 1-5 CPU/Memory board, Repeater Board, Fan, and Power Supply Indicator States

Power* (green)	Fault (amber)	OK to Remove† (amber)	Indication	Corrective Action
Off	Off	Off	Component not operating.	You can remove the component from the system.
Off	On	Off	Component not operating. Fault condition present.	You cannot remove the component from the system.
Off	Off	On	Component not operating. No fault condition present.	You can remove the component from the system.
Off	On	On	Component not operating. Fault condition present.	You can remove the component from the system.
On	Off	Off	Normal component operation.	N/A
On	Off	On	Component not operating. No fault condition present.	You can remove the component from the system.
On	On	Off	Component operating. Fault condition present.	You cannot remove the component from the system.
On	On	On	Component operating. Fault condition present.	You can remove the component from the system.

* Not applicable to fans.

† Not applicable to power supplies or fans.

Note – For power supplies, as long as a minimum of two power supplies are powered (with only the Power LED lit) one of the the other power supplies can be removed.

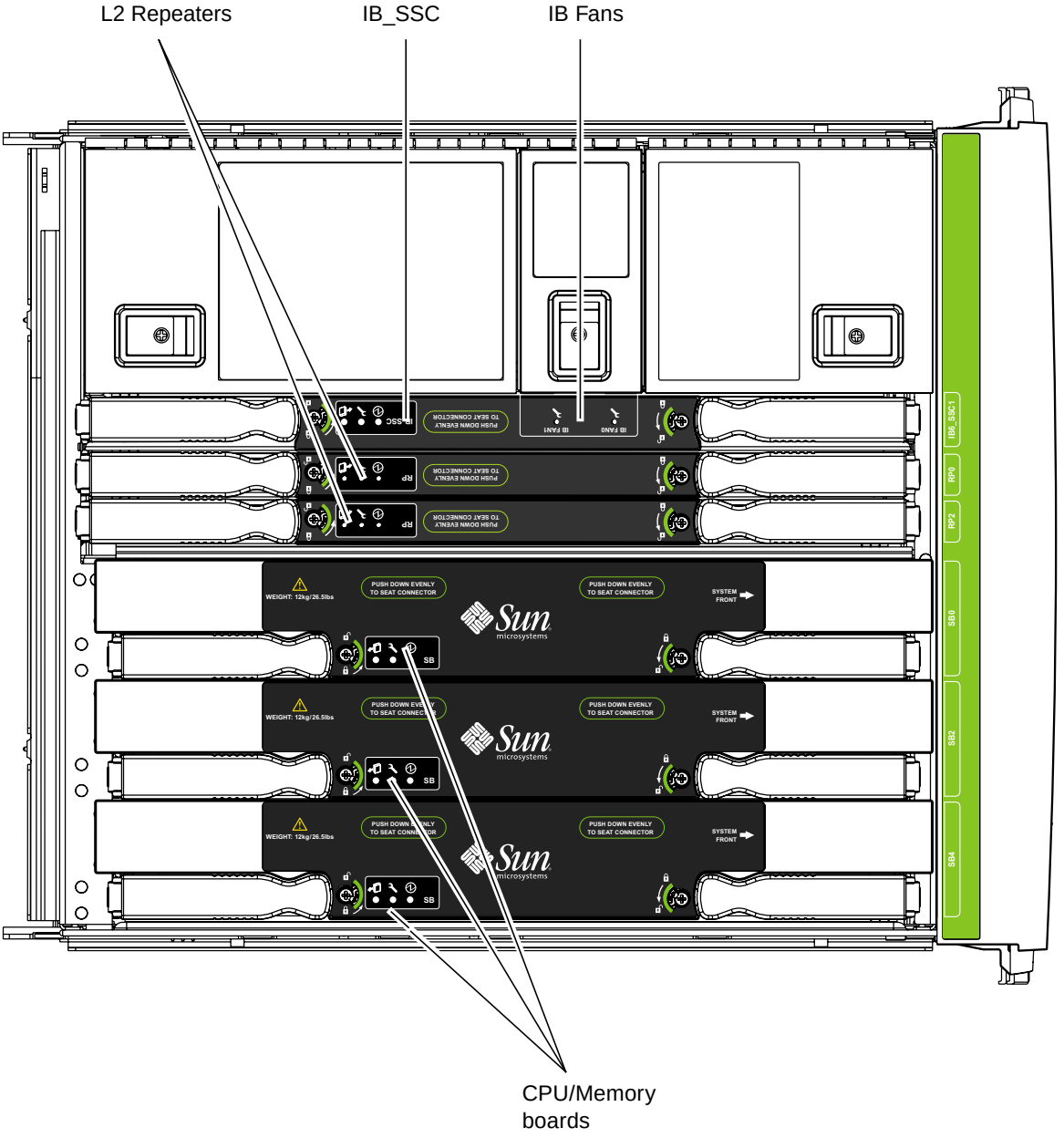


FIGURE 1-4 Locations of Modules and Indicator LEDs – Top of System

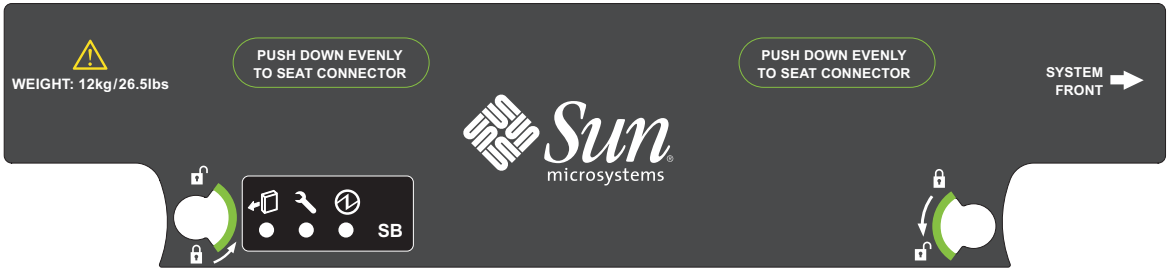


FIGURE 1-5 CPU/Memory board Indicator LEDs

FIGURE 1-6 L2 Repeater Indicator LEDs

FIGURE 1-7 IB_SSC and IB Fan Indicator LEDs

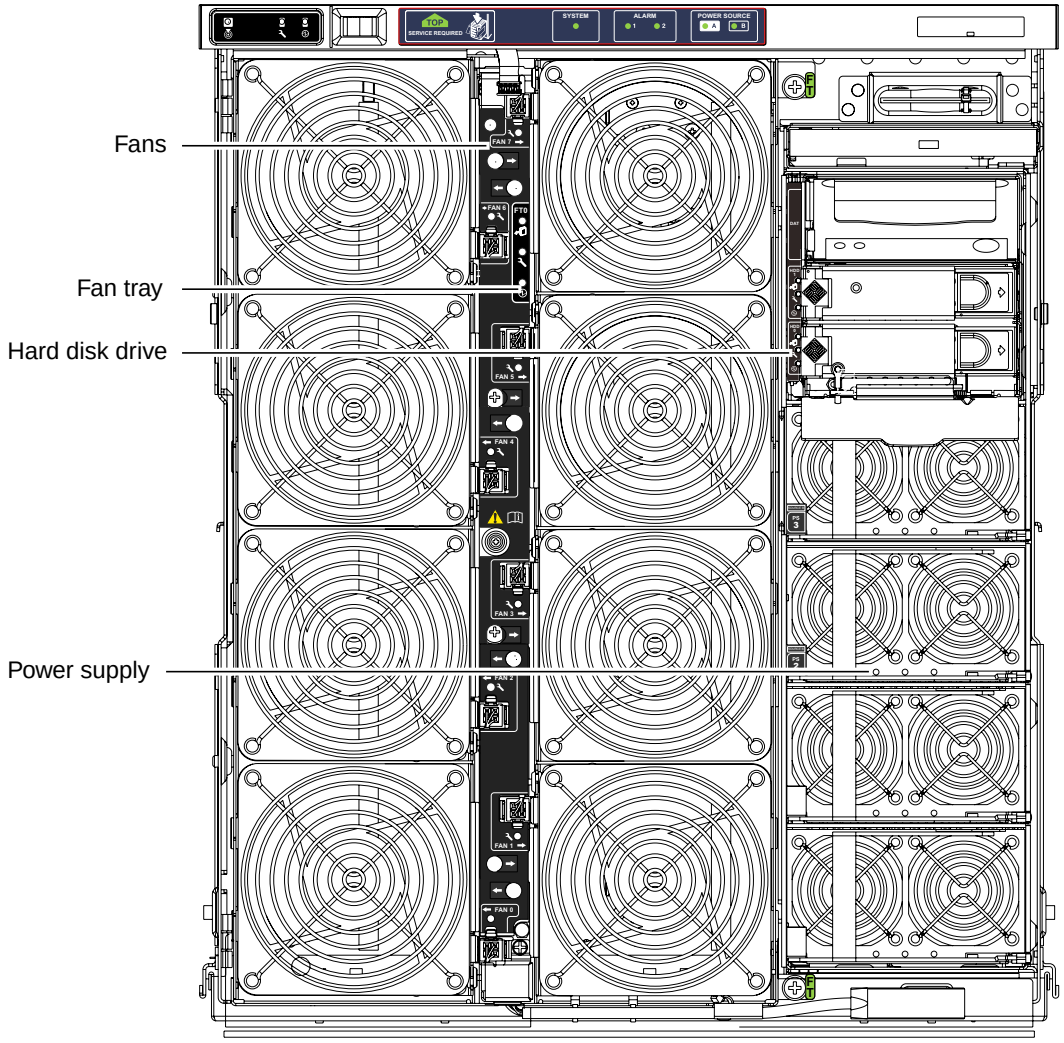


FIGURE 1-8 Module Indicator LED Locations – Front of System

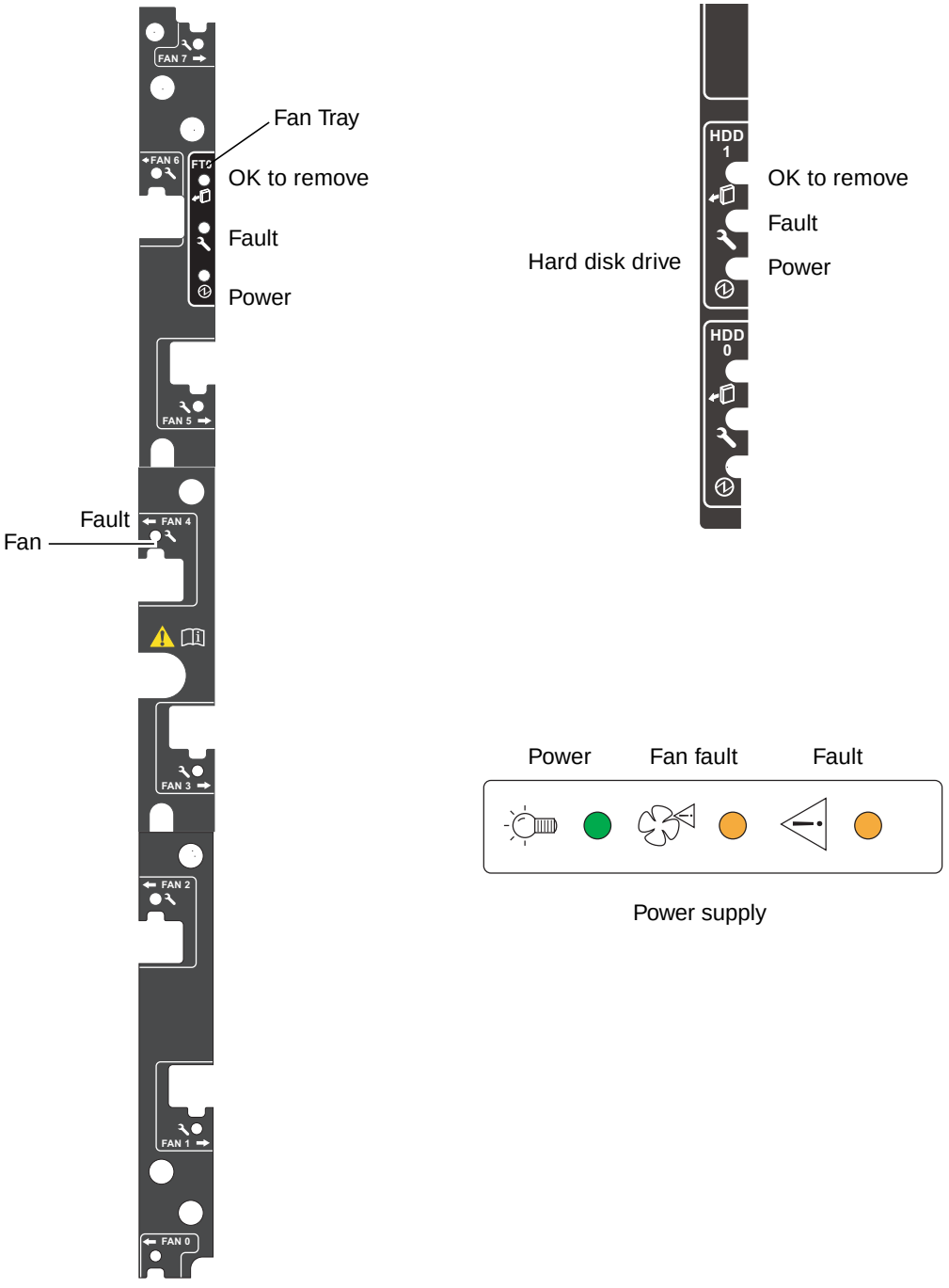


FIGURE 1-9 Power Supply, Hard Disk Drive, Fan and Fan Tray Indicator LEDs

1.4.3 Dynamic Reconfiguration (DR)

With the DR software, which is part of the Solaris operating environment, you can dynamically reconfigure CPU/Memory boards in order to safely remove them or install them into a system while the Solaris operating environment is running and with minimum disruption to user processes running in the system. The process of replacing a board while the system is still running is called hot-plugging. DR provides this software hot-plug support.

You can use DR to do the following:

- Shorten the interruption of system applications while installing or removing a board
- Disable a failing device by removing it from the logical configuration, before the failure can crash the operating system
- Display the operational status of boards in a system
- Initiate system tests of a board while the system continues to run
- Reconfigure a system while the system continues to run
- Invoke hardware-specific functions of a board or a related attachment

The DR software has a command line interface using the `cfgadm` command, which is the configuration administration program. The DR agent also provides a remote interface to the Sun Management Center software.

A DR operation has three distinct steps:

- Dynamic detach
- Hot replace
- Dynamic attach

For instructions on how to use the DR software, refer to the *Sun Fire V1280 System Administration Guide*.

1.4.4 Automatic System Reconfiguration (ASR)

Automatic system reconfiguration is a feature of the System Controller software that runs whenever a configuration is performed. The System Controller software checks for any recorded faults and configures hardware to exclude failed components in a configuration.

When the system fails, the system software brings the system back up as fast as possible with automatic system reconfiguration. However, an unassisted system reboot will not always be possible. For example, when a SCSI controller fails, the boot disk or the network connection may be lost.

You can use the multi-pathing feature, such as Alternate Pathing (AP), to extend the usefulness of automatic system reconfiguration.

There are two types of automatic system reconfiguration action, simple and partial.

1.4.4.1 Simple Automatic System Reconfiguration

Simple automatic system reconfiguration involves the removing a failed device from the system configuration. For example, if the DC to DC converter fails on the CPU/Memory board, the CPU/Memory board is removed.

1.4.4.2 Partial Automatic System Reconfiguration

Partial automatic system reconfiguration involves the partial deconfiguration of components on a board. The rest of the board can participate with a low risk of problems resulting from the failed parts.

1.4.5 Sun Management Center

The Sun Management Center program monitors system functioning and features a graphical user interface (GUI) to continuously display system status. The available functionalities will decrease significantly with a System Controller that is not networked. In order to provide the Sun Management Center global view of the chassis, access to the System Controller is required. With a networked System Controller Sun Management Center provides the following:

- Hardware information and monitoring of the entire chassis
- Photo-realistic images of the hardware
- Propagation of alarms to all associated components
- Environmental monitoring such as temperatures, fan status, and power supply condition

Refer to the *Sun Management Center Software User's Guide* for starting and operating instructions.

1.4.6 SunSolve OnLine

SunSolve Online is an informational and patch database service. It is used by system administrators, network administrators, and others who are responsible for maintenance of Sun hardware and software. There is also information for diagnosing and resolving problems with your Sun hardware and software. It contains proactive alerts for avoiding problems before they happen, and it provides helpful hints and guides for getting the most out of your Sun hardware and software.

SunSpectrum Contract customers have access to the entire SunSolve informational and patch database. For information about obtaining a SunSpectrum Contract, please contact your Sun Sales Rep or call 1-800-USA-4SUN. For access to SunSolve OnLine use the following URL: `http://sunsolve.Sun.com`.

1.4.7 OpenBoot

OpenBoot firmware is executed immediately after you turn on the system. The primary tasks of OpenBoot firmware are:

- Testing and initializing the system hardware
- Determining the system hardware
- Booting the operating system
- Providing interactive debugging facilities for testing hardware and software

For more information refer to the *OpenBoot 3.x Command Reference* manual.

1.4.8 Other Utilities

More information can be obtained using the following commands.

1.4.8.1 Solaris `prtfru` Command

The `prtfru` utility is used to obtain FRUID data from the system. Its output is a tree structure echoing the path in the FRU (Field-Replaceable Unit) tree to each container. When a container is found, the data from that container is printed in a tree-like structure as well. Refer to the `prtfru` manpage and Solaris documentation for more details.

1.4.8.2 System Controller `inventory` Command

Shows the contents of a FRU SEPROM.

Refer to the *Sun Fire V1280 System Controller Command Reference Manual* for more details.

PART II Preparing for Service

CHAPTER 2

Safety and Tool Requirements

This chapter describes the safety and system precautions you must take when servicing the system. It also lists the tools and equipment you will need.

Note – Many illustrations in this manual show the front doors removed. This is simply for clarity – it is not always necessary to remove the doors to carry out service actions.

2.1 Safety Precautions

For your protection, observe the following safety precautions when setting up your equipment:

- Follow all cautions, warnings, and instructions marked on the equipment.
- Never push objects of any kind through openings in the equipment as they may touch dangerous voltage points or short out components that could result in fire or electric shock.
- Refer servicing of equipment to qualified personnel.

To protect both yourself and the equipment, observe the following safety precautions:

TABLE 2-1 Safety Precautions

Item	Problem	Precaution
ESD jack / wrist or foot strap	Electro-Static Discharge (ESD)	The system has a number of ESD connections. Connect the ESD connector to your system and wear the wrist strap or foot strap when handling printed circuit boards.
ESD mat	ESD	An approved ESD mat provides protection from static damage when used with a wrist strap or foot strap. The mat also cushions and protects small parts that are attached to printed circuit boards.

2.2 Symbols

TABLE 2-2 Symbols

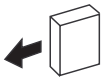
Symbol	Description	Meaning
	**CAUTION**	Hazardous voltages are present. To reduce the risk of electrical shock and danger, follow the instructions.
	**CAUTION**	Risk of personal injury. To reduce the risk, follow the instructions.
	**CAUTION**	Risk of equipment damage. To reduce the risk, follow the instructions.
	**HOT SURFACE**	CAUTION: Hot surfaces. Avoid contact. Surfaces are hot and may cause personal injury if touched.
	**COMPONENT ACTIVE**	Component or system is active when the green Active LED is lit.
	**OK TO REMOVE**	You can safely remove board or component from the system when the OK to Remove LED (amber) is lit.

TABLE 2-2 Symbols *(Continued)*

Symbol	Description	Meaning
	**FAULT**	The component or system has a fault when the Fault LED (amber) is lit,
	**PROTECTIVE EARTH**	Protective ground.
	**CHASSIS**	Frame or chassis ground.

2.3 System Precautions

Ensure that the voltage and frequency of the power outlet to be used matches the electrical rating labels on the equipment.

Wear antistatic wrist straps when handling any magnetic storage devices, system boards, or other printed circuit boards.

Use only properly grounded power outlets as described in the installation guide.

Caution – DO NOT make mechanical or electrical modifications. Sun Microsystems™ is not responsible for regulatory compliance of modified systems.

Caution – The chassis AC power cord(s) must remain connected to ensure a proper ground.

2.4 Handling Boards and Assemblies

Caution – There is a separate chassis ground located on the rear of the system. It is important to ensure that the system is properly grounded.

Caution – The system is sensitive to static electricity. To prevent damage to the board, connect an antistatic wrist strap between you and the system.

Caution – The boards have surface-mount components that can be broken by flexing the boards.

To minimize the amount of board flexing, observe the following precautions:

- Hold the board only by the handle and by the green fingerhold panels, where the board stiffener is located. Do not hold the board *only* at the ends.
- When removing the board from an antistatic bag, keep the board vertical until you lay it on the ESD mat.
- Do not place the board on a hard surface. Use a cushioned antistatic mat. The board connectors and components have very thin pins that bend easily.
- Be careful of small component parts located on both sides of the board.
- Do not use an oscilloscope probe on the components. The soldered pins are easily damaged or shorted by the probe point.
- Transport the board in an antistatic bag.

Caution – The heatsinks can be damaged by incorrect handling. Do not touch the heatsinks while replacing or removing boards. If a heatsink is loose or broken, obtain a replacement board.

Caution – The heatsinks can be damaged by improper packaging. When storing or shipping a board, ensure that the heatsinks have sufficient protection.

2.5 Filler Boards and Filler Panels

Filler boards and panels, which are physically inserted into the board or card slot, are used for EMI protection and for air flow.

In order to prevent the system from overheating when you remove a CPU/Memory board from a system, install a filler board.

In order to provide full EMI protection, ensure that filler panels are installed when removing the tape drive or a PCI card, and filler boards to replace CPU/Memory boards when they are permanently removed.

2.6 Antistatic Precautions

Caution – Wear an antistatic wrist strap and use an ESD-protected mat when handling components. When servicing or removing system unit components, use an antistatic wrist strap with a 10mm press stud connection and attach the antistatic wrist strap to the press stud at the rear or side of the chassis before removing any covers or components.

There are three antistatic strap attachment points on the chassis:

- Left-hand side towards the front; refer to FIGURE 2-1
- Right-hand side towards the front; refer to FIGURE 2-2
- Center at the rear
- Center of the fan tray, at the front.

- **To attach the antistatic wrist strap to the chassis, connect the strap as shown in** FIGURE 2-1 **or** FIGURE 2-2**.**

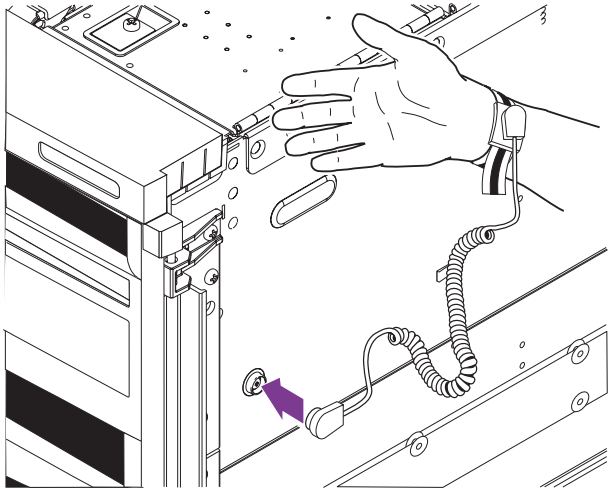


FIGURE 2-1 Attaching the Antistatic Wrist Strap – Right-Hand Side

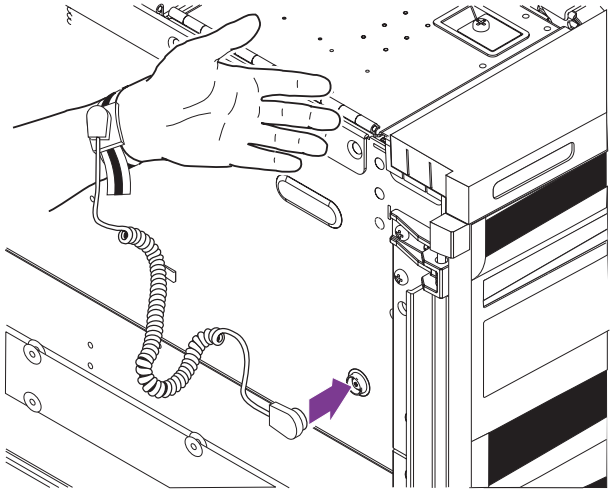


FIGURE 2-2 Attaching the Antistatic Wrist Strap – Left-Hand Side

2.7 Tools Required

For the procedures in this document, you will need these tools:

- Screwdriver, Phillips #2
- Screwdriver, Phillips #2 with short shank (‘stubby’) (baseplane removal)
- Needlenose pliers (connector removal)
- ESD mat
- ESD grounding wrist strap or foot strap

CHAPTER 3

Powering On and Off

This chapter explains how to power the system on and off, and how to transition between the various system states.

These states are:

- Powered down completely (no power applied to the system)
- Standby (power applied but only the System Controller and associated components are active)
- Powered on (power applied and the system active)

3.1 Using the Power (On/Standby) Switch

Caution – The power switch is not an On/Off switch, it is an On/Standby switch. It does not isolate the equipment.

The power (On/Standby) switch of the Sun Fire V1280 server is a rocker type, momentary action switch. It controls only low voltage signals and no high voltage circuits pass through it.

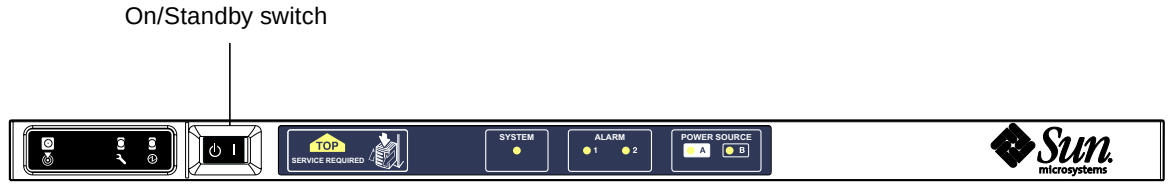


FIGURE 3-1 Sun Fire V1280 Server Power (On/Standby) Switch04

The symbols on the switch are:

| On

Press and release to power on the server. This is the equivalent of the LOM `poweron` command.

⏻ Standby

Press for less than four seconds to initiate an orderly shutdown of the system into Standby mode. This is equivalent to issuing the `shutdown` command at the `lom>` prompt. This is the method to use under normal operation.

Press and hold down for more than four seconds to perform a system power down to standby mode. This is equivalent to issuing the `poweroff` command at the `lom>` prompt. This process is not interruptible.

Note – You should ensure that Solaris is cleanly shut down before powering a system to standby mode otherwise data is at risk of being lost.

Use the LOM `setupsc` command to prevent accidental operation of the On/Standby switch.

3.2 Powering On

3.2.1 Initial Power-On

1. **Ensure all power cables are connected and external circuit breakers are switched on.**
2. **The system will enter Standby mode.**

   The only indicator LEDs to be illuminated on the system indicator board are the Source A and Source B indicators. The IB_SSC assembly Power LED will also be illuminated, but not visible from the front of the system.

Note – Fan 3 is the only fan that will be powered up.

3.2.2 Powering On from Standby Mode

Powering the system on from Standby mode can be achieved in either of two ways:

- Operating the On/Standby switch
- Sending the `poweron` command via the LOM port.

If the `auto-boot?` variable has been set in the OBP, the system will automatically boot into the Solaris operating environment.

3.2.2.1 Using the On/Standby Switch

1. **Check that power is applied to the system and that it is correctly in Standby mode.**

   The only indicator LEDs to be illuminated on the system indicator board are the Source A and Source B indicators. The IB_SSC assembly Active LED will also be illuminated, but not visible from the front of the system.

2. **Momentarily press the On/Standby switch to the right.**

   The system will power on completely. The System Active indicator will be illuminated in addition to the Source A and Source B indicators. The system will execute the power on self tests (POST).

3.2.2.2 Using the LOM `poweron` Command

- **At the `lom>` prompt, type:**

```
lom>poweron
```

The system will power on completely. The System Active indicator will be illuminated in addition to the Source A and Source B indicators. The system will execute the power on self tests (POST).

Note – The `poweron all` command only powers on the system boards; it does not boot Solaris.

Refer to the *Sun Fire V1280 System Controller Command Reference Manual* for a full description of the `poweron` command.

3.3 Powering Off

3.3.1 Bringing the System to Standby Mode

This can be achieved in one of five ways:

- Using the UNIX `shutdown` command.
- Sending the `shutdown` command via the LOM port
- Sending the `shutdown` command using the On/Standby switch
- Sending the `poweroff` command via the LOM port
- Sending the `poweroff` command using the On/Standby switch

Note – You should ensure that Solaris is cleanly shut down before powering a system to standby mode otherwise data is at risk of being lost.

Note – Fan 3 is the only fan that will remain in operation in Standby mode.

Note – If an unrecoverable hardware error occurs that results in Solaris being stopped, the system should be powered off using the `poweroff` command at the LOM prompt before attempting to bring Solaris back into service using the `poweron` command.

3.3.1.1 Using the Solaris `shutdown` Command

- **At the system prompt, type:**

```
# shutdown -i5
```

The system will power off to standby mode. The only indicator LEDs to be illuminated on the system indicator board are the Source A and Source B indicators. The IB_SSC assembly Active LED will also be illuminated, but not visible from the front of the system.

3.3.1.2 Sending the LOM shutdown Command

Note – If Solaris is running this command will attempt to halt the system cleanly before powering down the system to standby mode, and is the equivalent of the Solaris `init 5` command.

- **At the** `lom>` **prompt, type:**

```
lom>shutdown
```

After Solaris has been stopped, the system will power off to standby mode. The only indicator LEDs to be illuminated on the system indicator board are the Source A and Source B indicators. The IB_SSC assembly Active LED will also be illuminated, but not visible from the front of the system.

Refer to the *Sun Fire V1280 System Controller Command Reference Manual* for a full description of the LOM `shutdown` command.

3.3.1.3 Sending the shutdown Command Using the On/Standby Switch

- **Momentarily press the system On/Standby switch to the left.**

  This initiates an orderly shutdown of the system into Standby mode. This is equivalent to issuing the `shutdown` command at the `lom>` prompt.

3.3.1.4 Sending the LOM poweroff Command

- **At the** `lom>` **prompt, type:**

```
lom>poweroff

This will abruptly terminate Solaris.
Do you want to continue? [no]
```

Type **y** to continue or press Return to cancel the command.

The system will power off to standby mode. The only indicator LEDs to be illuminated on the system indicator board are the Source A and Source B indicators. The IB_SSC assembly Active LED will also be illuminated, but not visible from the front of the system.

Refer to the *Sun Fire V1280 System Controller Command Reference Manual* for a full description of the `poweroff` command.

3.3.1.5 Sending the `poweroff` Command Using the On/Standby Switch

- **Press the On/Standby switch to the left and hold it for at least four seconds.**

  The system will power down to standby mode. The only indicator LEDs to be illuminated on the system indicator board are the Source A and Source B indicators. The IB_SSC assembly Active LED will also be illuminated, but not visible from the front of the system.

PART III Subassembly Removal and Replacement

CHAPTER 4

Storage Devices

This chapter describes how to remove and install hard disk, tape and DVD drives, the SCC reader, and the removable media bay. It contains the following sections:

The hard disk drives can be removed and installed without powering off the system. The removable media drives and bay can only be removed after powering off the system.

4.1 Hard Disk Drives

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

4.1.1 To Remove a Hard Disk Drive

1. **Ensure the disk is backed up and unconfigured, and that the OK to Remove LED is lit.**

   Refer to FIGURE 1-9.

2. **Open the right-hand front door of the system.**

3. **Attach a wrist strap or foot strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system. Place a grounded ESD mat close to the system.

4. **Lower the grille in fromt of the hard disk drives.**

5. **Push the handle latch to the right to open the drive handle.**

   Refer to FIGURE 4-1.

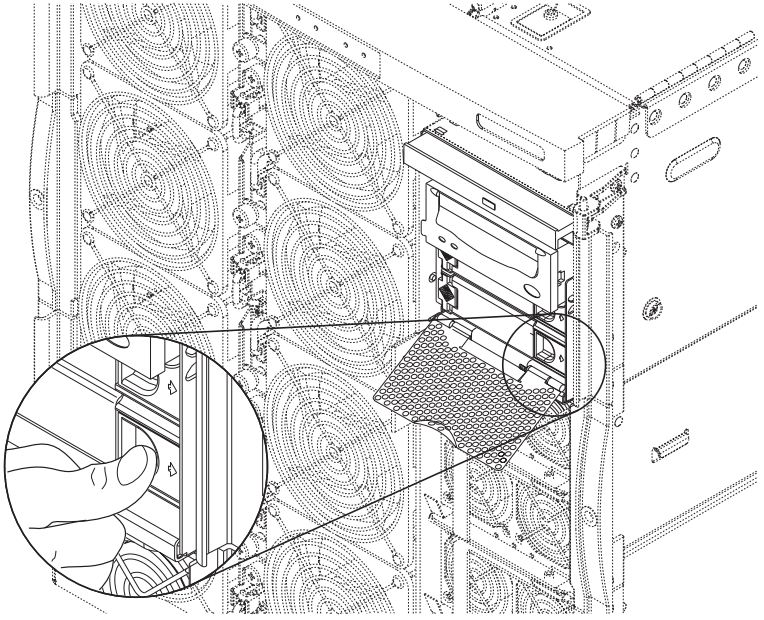


FIGURE 4-1 Releasing the Hard Disk Drive Ejector

6. Extend the drive handle to disconnect the drive from the system.

Refer to FIGURE 4-2.

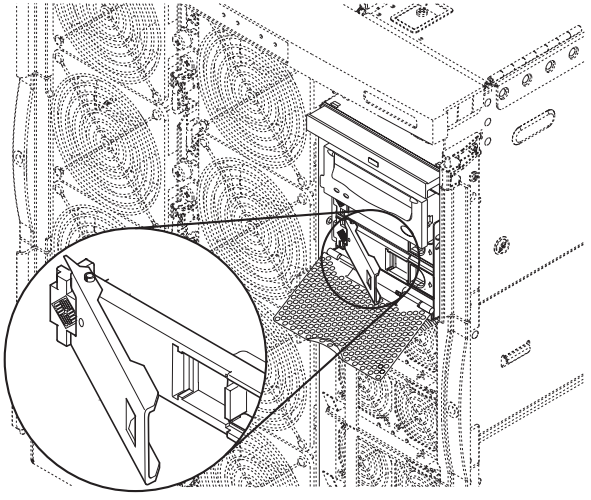


FIGURE 4-2 Ejecting the Hard Disk Drive

7. **Holding the drive handle and pull the drive from the drive bay.**

   The hard disk drive rear connector is disconnected when the drive is ejected. Refer to FIGURE 4-3.

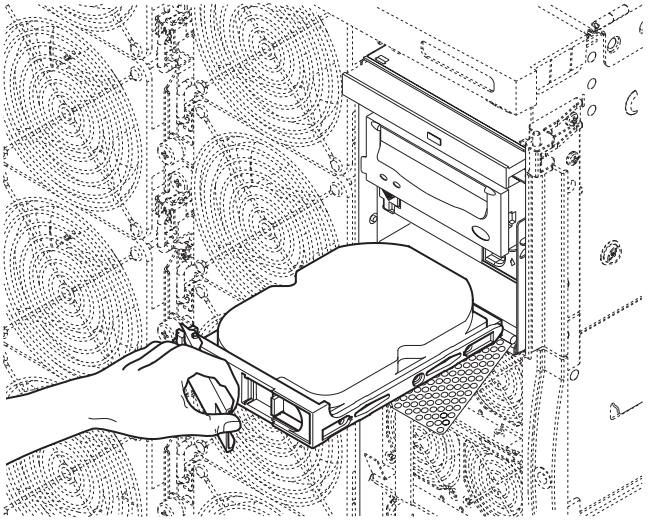


FIGURE 4-3 Removing the Hard Disk Drive

8. **Place the drive on an ESD mat.**
9. **If required, replace the drive as described in "To Install a Hard Disk Drive" on page 4-4.**
10. **Detach the antistatic wrist strap.**
11. **Close the front door of the system.**
12. **Reconfigure if necessary, and ensure that the LEDs are no longer lit.**

4.1.2 To Install a Hard Disk Drive

1. **Open the right-hand front door of the system**
2. **Attach a wrist strap or foot strap.**

   Refer to Section 2.6, "Antistatic Precautions" on page 2-5. Connect the ESD wrist strap or foot strap to the system.

3. **Lower the grille in front of the hard disk drives.**
4. **Push the hard disk drive into the bay as far as it will go.**

5. **Close the drive handle to connect the drive to the system.**
6. **Detach the antistatic wrist strap.**
7. **Close the front door of the system.**
8. **Reconfigure if necessary, and ensure that the LEDs are no longer lit.**

4.2 Tape Drive

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

Caution – This procedure requires the system to be extended out of the rack on its slides. Before attempting this procedure you must deploy rack stabilization devices, if fitted.

Note – The tape drive has a SCSI ID of 5.

4.2.1 Replacing an Existing Tape Drive

1. **Power off the system to standby.**

   Refer to Section 3.3, “Powering Off” on page 3-4.

2. **Deploy the rack stabilization device, if fitted.**
3. **Extend the system from the rack.**

   Loosen the captive screws securing the system to the rack and gently pull it out on its slides.

4. **Open the right-hand front door of the system.**
5. **Attach a wrist strap or foot strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system. Place a grounded ESD mat close to the system.

6. **Open the media bay cover.**

   Loosen the latch securing screw, lift the latch and raise the cover. Refer to FIGURE 4-6.

7. **Remove the media bay.**

   Refer to Section 4.6.1, “To Remove the Media Bay” on page 4-18.

8. **Hold the metal tab on the left of the DAT drive to the left and pull out the drive.**

9. **Place the drive on an ESD mat.**

10. **If you are going to install a new drive, remove the four screws securing the baseplate to the drive and remove the baseplate.**

    Refer to FIGURE 4-5.

11. **Install the new drive by pushing it into the chassis until the metal latch on the left-hand side engages.**

    Refer to Section 4.2.2, “Installing a New Tape Drive” on page 4-6. If you do not install a tape drive you must install a filler module instead.

12. **Reinstall the media bay.**

    Refer to Section 4.6.2, “To Install the Media Bay” on page 4-20.

4.2.2 Installing a New Tape Drive

1. **Power off the system to standby.**

   Refer to Section 3.3, “Powering Off” on page 3-4.

2. **Deploy the rack stabilization device, if fitted.**

3. **Extend the system from the rack.**

   Loosen the captive screws securing the system to the rack and gently pull it out on its slides.

4. **Open the right-hand front door of the system.**

5. **Attach a wrist strap or foot strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system. Place a grounded ESD mat close to the system.

6. **Open the media bay cover.**

   Loosen the latch securing screw, lift the latch and raise the cover. Refer to FIGURE 4-6.

7. **Remove the DAT drive filler module by pulling it forwards.**

8. **Remove the front of the blank module by removing the two countersunk screws.**
   This part can be discarded. Refer to FIGURE 4-4.

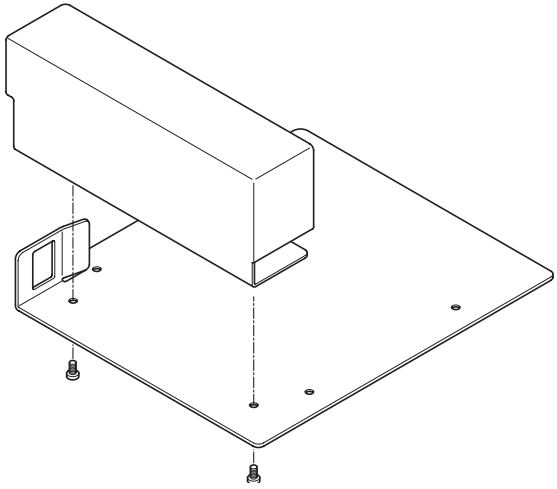


FIGURE 4-4 Dismantling the DAT Filler Panel

9. **Offer up the base plate from the blank module to the DAT tape drive.**

   Fix the base plate from the blank module to the DAT tape drive using the four countersunk screws shipped with the drive. Refer to FIGURE 4-5.

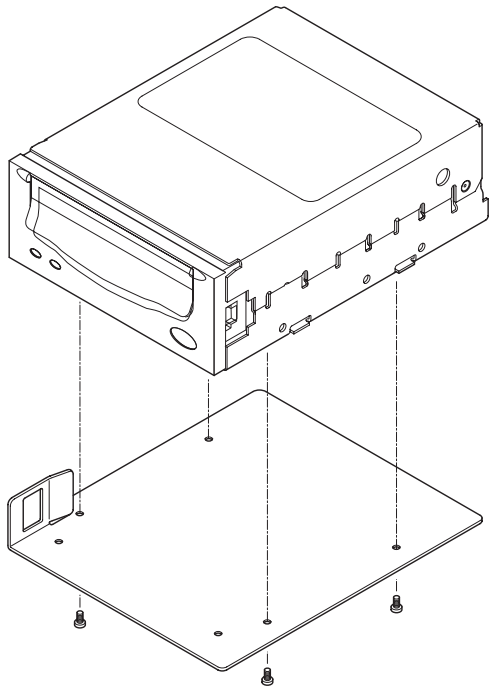


FIGURE 4-5 Assembling the DAT drive

10. **Pull out the media bay.**

    Refer to Section 4.6.1, “To Remove the Media Bay” on page 4-18.

11. **Install the new drive.**

    Refer to Section 4.2.1, “Replacing an Existing Tape Drive” on page 4-5.

12. **Reinstall the media bay and reconnect al the power and data cables.**

    Refer to Section 4.6.2, “To Install the Media Bay” on page 4-20.

13. **Close the media bay cover and tighten the latch securing screw.**

14. **Detach the antistatic wrist strap.**

15. **Close the front door of the system.**

16. **Slide the system back into the rack and secure it.**

17. **Retract the rack stabilization device, if fitted.**

18. **Power on the system.**

    Refer to Section 3.2, “Powering On” on page 3-2.

19. **Take the system down to the OpenBoot PROM** ok **prompt and type:**

```
ok boot -r
```

4.3 DVD-ROM Drive

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

Caution – This procedure requires the system to be extended out of the rack on its slides. Before attempting this procedure you must deploy rack stabilization devices, if fitted.

4.3.1 To Remove the DVD-ROM Drive

1. **Power off the system to standby.**

   Refer to Section 3.3, “Powering Off” on page 3-4.

2. **Deploy the rack stabilization device, if fitted.**

3. **Extend the system from the rack.**

   Loosen the captive screws securing the system to the rack and gently pull it out on its slides.

4. **Open the right-hand front door of the system.**

5. **Attach a wrist strap or foot strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system. Place a grounded ESD mat close to the system.

6. **Open the media bay cover.**

Loosen the latch securing screw, lift the latch and raise the cover. Refer to FIGURE 4-6.

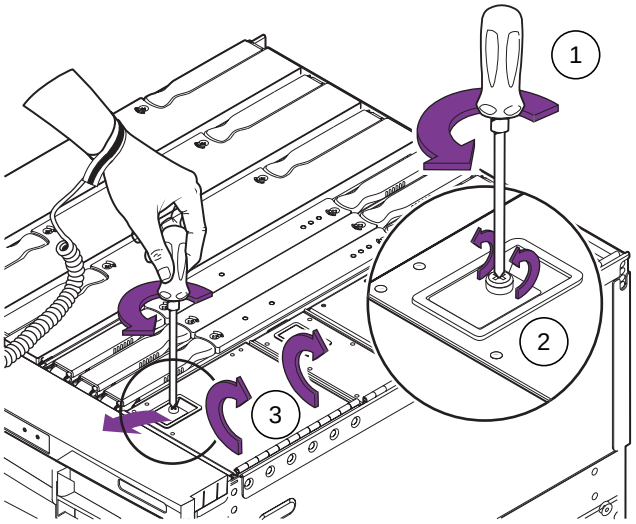


FIGURE 4-6 Opening the Media Bay Cover

7. **Inside the media bay, push the metal latch retaining the drive to the right.**

You can now withdraw the drive from the backplane connector by firmly pulling it from the front of the system. Refer to FIGURE 4-7.

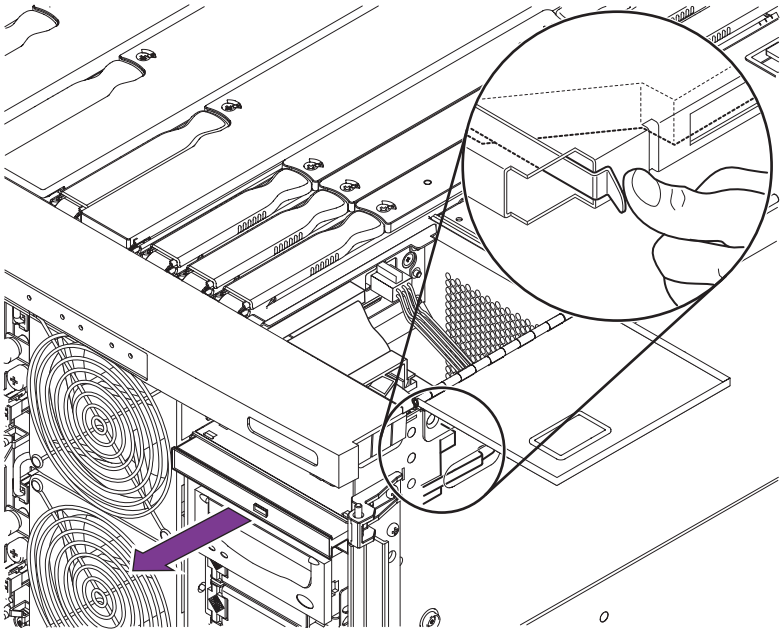


FIGURE 4-7 Removing the DVD-ROM Drive

8. **Place the drive on an ESD mat.**
9. **If required, install a new drive as described in “To Install the DVD-ROM Drive” on page 4-11.**
10. **Close the media bay cover and tighten the latch securing screw.**
11. **Detach the antistatic wrist strap.**
12. **Close the front door of the system.**
13. **Slide the system back into the rack and secure it.**
14. **Retract the rack stabilization device, if fitted.**

4.3.2 To Install the DVD-ROM Drive

1. **Power off the system to standby.**
   Refer to Section 3.3, “Powering Off” on page 3-4.
2. **Open the right-hand front door of the system.**

3. **Attach a wrist strap or foot strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system.

4. **Push the DVD-ROM drive into the chassis until the latch engages..**

5. **Detach the antistatic wrist strap.**

6. **Close the front door of the system.**

4.4 DVD-ROM Backplane

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

Caution – This procedure requires the system to be extended out of the rack on its slides. Before attempting this procedure you must deploy rack stabilization devices, if fitted.

1. **Power off the system to standby.**

   Refer to Section 3.3, “Powering Off” on page 3-4.

2. **Deploy the rack stabilization device, if fitted.**

3. **Extend the system from the rack.**

   Loosen the captive screws securing the system to the rack and gently pull it out on its slides.

4. **Open the right-hand front door of the system.**

5. **Attach a wrist strap or foot strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system. Place a grounded ESD mat close to the system.

6. **Open the media bay cover.**

   Loosen the latch securing screw, lift the latch and raise the cover. Refer to FIGURE 4-6.

7. **Inside the media bay, push the metal latch retaining the DVD-ROM drive to the right.**

   You can now withdraw the drive from the backplane connector by firmly pulling it from the front of the system. Refer to FIGURE 4-7.

8. **Unplug the DVD-ROM backplane connector from the IB_SSC.**
9. **Lift the DVD-ROM backplane out of its holder.**
10. **Insert the new DVD-ROM backplane and plug its connector into the IB_SSC.**
11. **Push the DVD-ROM drive into the chassis until the latch engages..**
12. **Detach the antistatic wrist strap.**
13. **Close the front door of the system.**
14. **Retract the rack stabilization device, if fitted.**

4.5 SCC Reader

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

Caution – This procedure requires the system to be extended out of the rack on its slides. Before attempting this procedure you must deploy rack stabilization devices, if fitted.

4.5.1 To Remove the SCC Reader

1. **Power off the system and remove the input power connector(s).**

   Refer to Section 3.3, “Powering Off” on page 3-4.

2. **Deploy the rack stabilization device, if fitted.**

3. **Extend the system from the rack.**

   Loosen the captive screws securing the system to the rack and gently pull it out on its slides.

4. **Attach a wrist strap or foot strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system. Place a grounded ESD mat close to the system.

5. **Remove the system configuration card.**

6. **Open the media bay cover.**

   Loosen the latch securing screw, release the latch and lift the cover open. Refer to FIGURE 4-6.

7. **Disconnect the IDE ribbon cable and the SCC reader cable.**

   Refer to FIGURE 4-8.

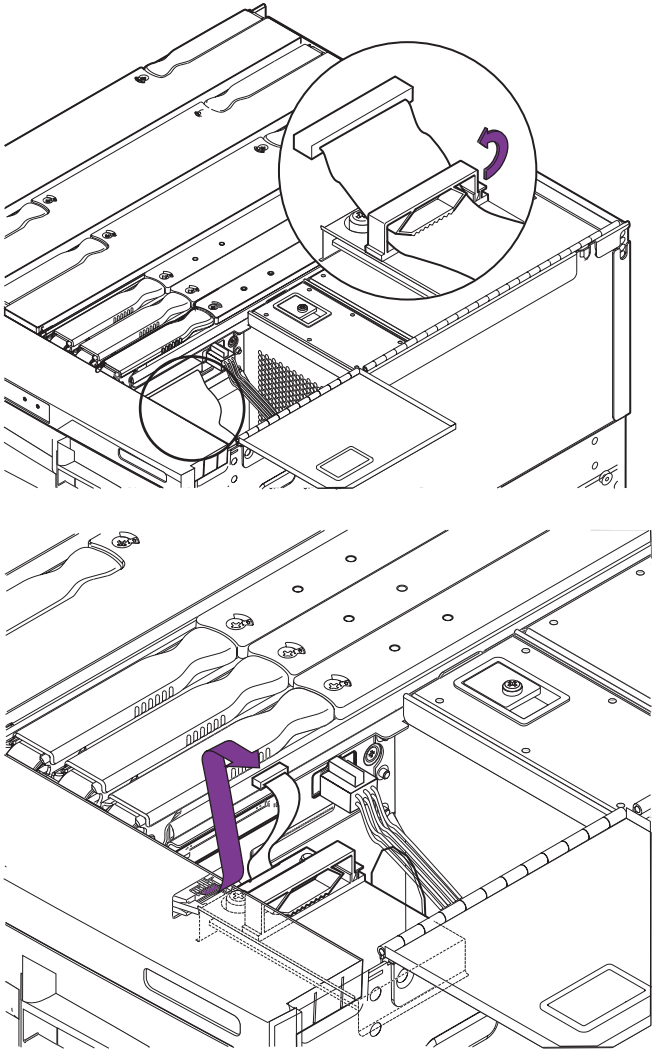


FIGURE 4-8 Disconnecting the SCCR Cables

8. **Loosen completely the captive screw securing the reader.**

Refer to FIGURE 4-9.

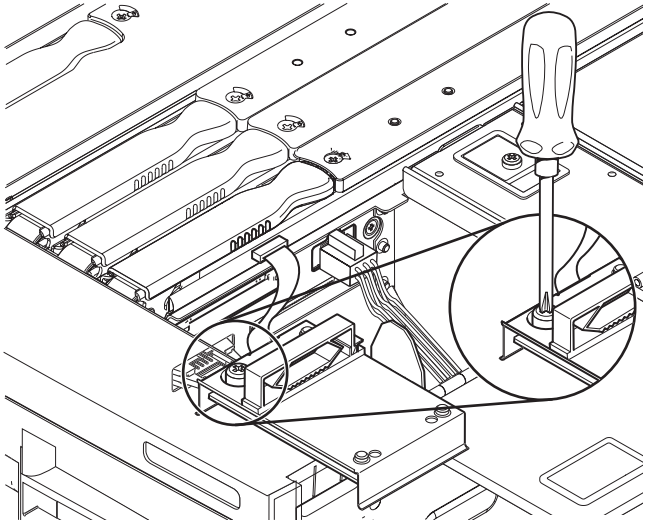


FIGURE 4-9 Loosening the SCC Reader Captive Screw

9. **Lift the reader off its locating pins and place it on an ESD mat.**

Refer to FIGURE 4-10.

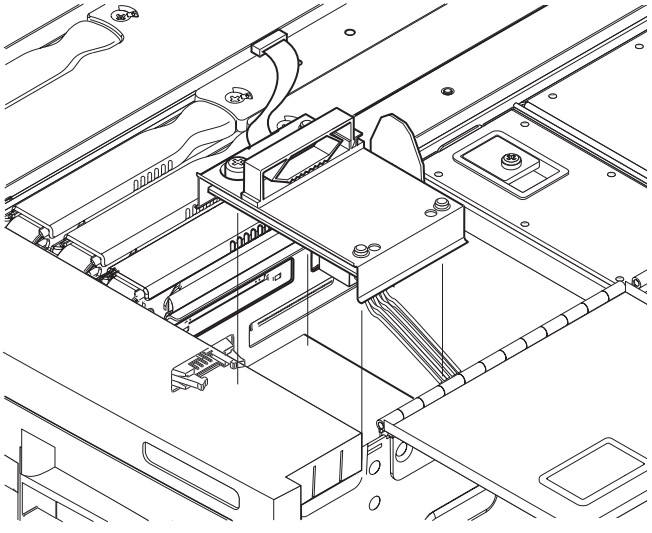


FIGURE 4-10 Removing the SCC Reader

4.5.2 To Install the SCC Reader

1. **Power off the system and remove the input power connector(s).**

   Refer to Section 3.3, “Powering Off” on page 3-4.

2. **Deploy the rack stabilization device, if fitted.**

3. **Extend the system from the rack.**

   Loosen the captive screws securing the system to the rack and gently pull it out on its slides.

4. **Attach a wrist strap or foot strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system. Place a grounded ESD mat close to the system.

5. **Open the media bay cover.**

   Loosen the latch securing screw, release the latch and lift the cover open.

6. **Connect the SCC reader cable.**

7. **Place the reader over its locating pins and press firmly to seat it.**

8. **Tighten the securing screw fully.**

9. **Close and latch the media bay cover.**

10. **Remove the wrist strap.**

11. **Slide the system into therack and secure it.**

12. **Retract the rack stabilization device, if fitted.**

4.6 Removable Media Bay

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

Caution – This procedure requires the system to be extended out of the rack on its slides. Before attempting this procedure you must deploy rack stabilization devices, if fitted.

4.6.1 To Remove the Media Bay

1. **Power down the system and remove the input power connectors.**

   Refer to Section 3.3, “Powering Off” on page 3-4.

2. **Deploy the rack stabilization device, if fitted.**

3. **Extend the system from the rack.**

   Loosen the captive screws securing the system to the rack and gently pull it out on its slides.

4. **Open the right-hand front door.**

5. **Attach a wrist strap or foot strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system. Place a grounded ESD mat close to the system.

6. **Open the media bay cover.**

   Loosen the latch securing screw, lift the latch and raise the cover. Refer to FIGURE 4-6.

7. **Remove the cables from the SCC reader, tape drive and hard disk drives to the IB_SSC assembly.**

   You may also need to remove the foam airflow filter in front of the IB fan intake. Refer to Section 4.1.1, “To Remove a Hard Disk Drive” on page 4-2, Section 4.5.1, “To Remove the SCC Reader” on page 4-14 and FIGURE 4-11.

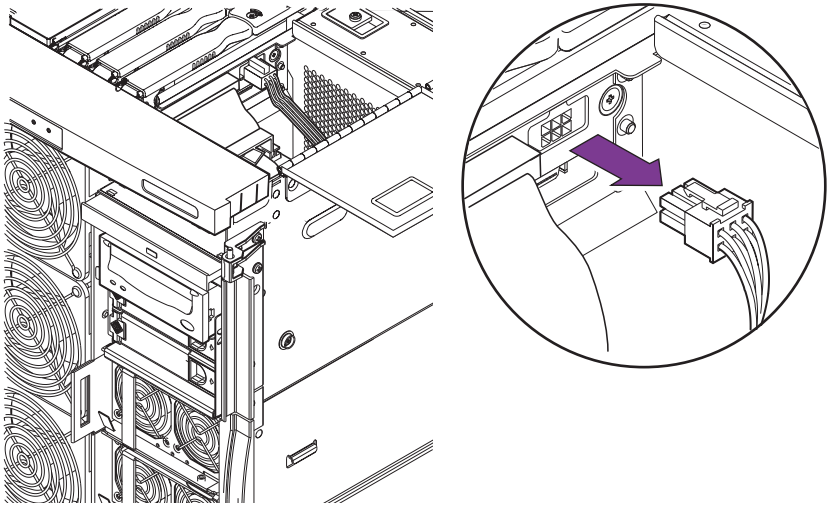


FIGURE 4-11 Removing Cables from the IB_SSC Assembly to the Media Bay

8. **Locate the convex spring behind the right-hand side of the media bay and press it in so it becomes concave.**

   Refer to FIGURE 4-12.

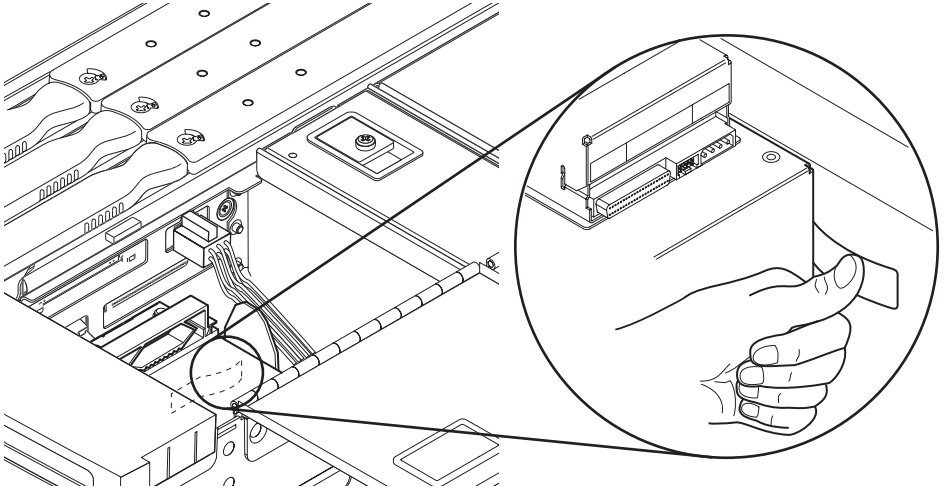


FIGURE 4-12 Releasing the Media Bay Retaining Spring

9. **Grasping the metal blade at the front, withdraw the media bay a short distance from the system chassis.**

   Refer to FIGURE 4-13.

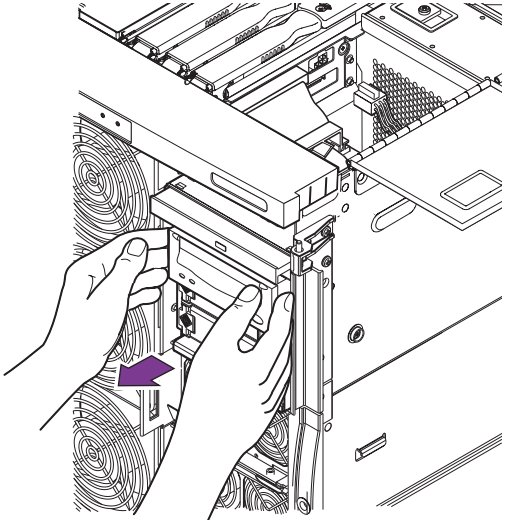


FIGURE 4-13 Pulling Out the Media Bay a Short Distance

10. **Unplug the tape drive connectors.**

    Refer to Section 4.2, “Tape Drive” on page 4-5.

11. **Fully withdraw the media bay, ensuring that the connectors and cables do not catch on anything.**

    Refer to FIGURE 4-14.

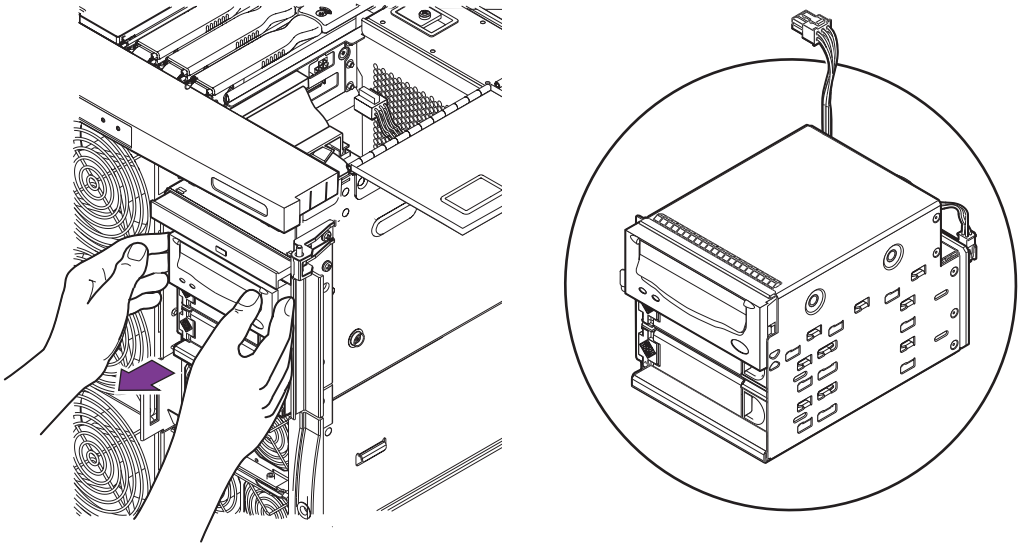


FIGURE 4-14 Removing the Media Bay

12. **Place the chassis on an ESD mat.**

4.6.2 To Install the Media Bay

1. **Open the front right-hand door of the system.**
2. **Insert the chassis into the system a short way.**
3. **Reconnect the tape drive connectors.**
4. **Push the media bay fully home until the metal tag engages.**
5. **Reconnect the remaining cables.**
6. **Remove the wrist strap.**
7. **Slide the system into the rack and secure it.**

8. Retract the rack stabilization device, if fitted.

CHAPTER 5

Cooling Subsystem

This chapter describes how to remove and install the main system fans and fan tray, and the IB fans.

Individual fans can be replaced without powering down the system. Replacing the main fan tray requires that the system be powered down.

5.1 Main Fans

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

Caution – Do not operate for extended periods with a fan removed. Doing so may cause system shutdown.

5.1.1 To Remove a Main Fan

1. **Open the front doors of the system.**
2. **Attach the wrist strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5.
3. **Identify the power connector and retaining screw of the fan to be removed.**

   The fan’s Fault LED should be illuminated. Refer to FIGURE 1-9.

4. **Unplug the appropriate power connector.**

   Refer to FIGURE 5-1.

Caution – You should wait at least ten seconds before proceeding to allow the fan to stop spinning.

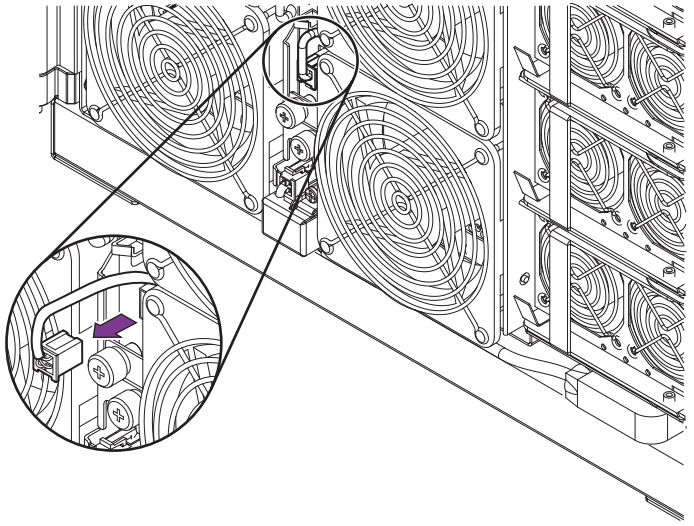


FIGURE 5-1 Unplugging the Fan Power Connector

5. **Unscrew the appropriate captive screw retaining the fan.**

Caution – There is no finger guard on the reverse side of the fan. Take care to hold the fan only by the sides of the assembly.

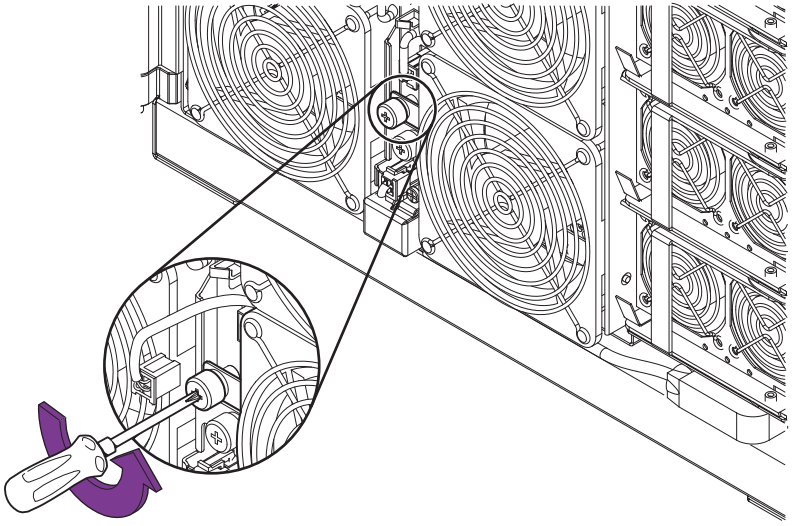


FIGURE 5-2 Loosening the Fan Retaining Screw

6. Remove the fan and place on an ESD mat.

Refer to FIGURE 5-3.

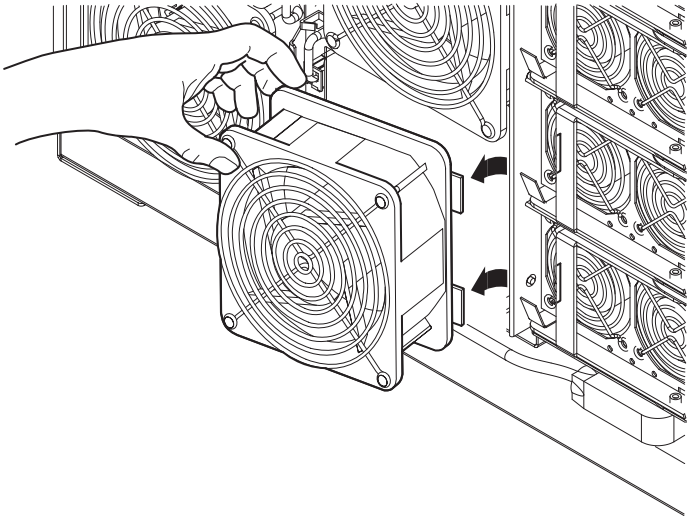


FIGURE 5-3 Removing a Fan

5.1.2 To Install a Main Fan

1. **Open the front doors of the system.**
2. **Attach a wrist or foot strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5.
3. **Orient the fan so that the two lugs on the metal carrier will engage in the cutouts in the fan tray.**
4. **Tighten the captive screw to retain the fan.**
5. **Plug in the fan power connector.**

   If the system is powered on the fault LED will be extinguished.

Note – If a fan has failed and the system shut down to Standby, the fault indicator will not be extinguished until the system is powered on again.

Caution – If the system is powered up, or the newly-installed fan is Fan 3, the fan will start immediately it is plugged in.

5.2 Main Fan Tray

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

5.2.1 To Remove the Fan Tray

1. **Power off the system and remove the input power connector(s).**

   Refer to Section 3.3, “Powering Off” on page 3-4.
2. **Open the front doors of the system.**
3. **Attach the wrist strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5.

4. **Unlatch and unplug the fan tray power connector.**

   Refer to FIGURE 5-4.

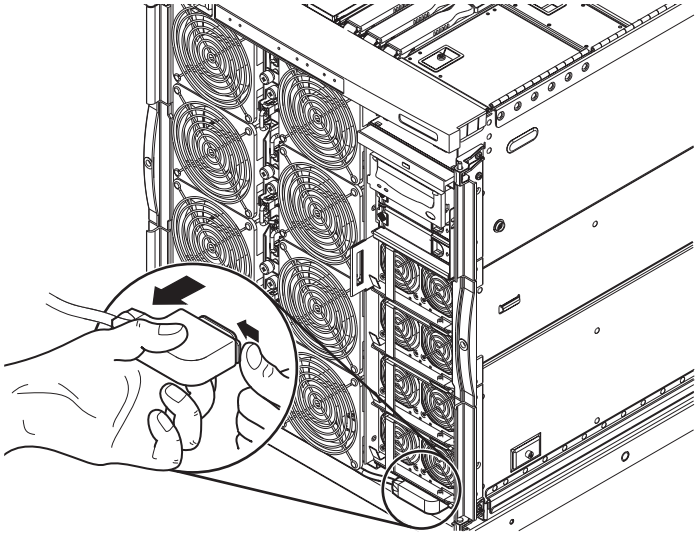


FIGURE 5-4 Removing the Fan Tray Power Connector

5. **Remove the system indicator board connector retaining clip and unplug the connector.**

   Refer to Section 10.1, “Removing the System Indicator Board” on page 10-1.

6. **Unscrew the two captive screws retaining the fan tray.**

   There is one at the top and one at the bottom right-hand side of the fan tray. Refer to FIGURE 5-5.

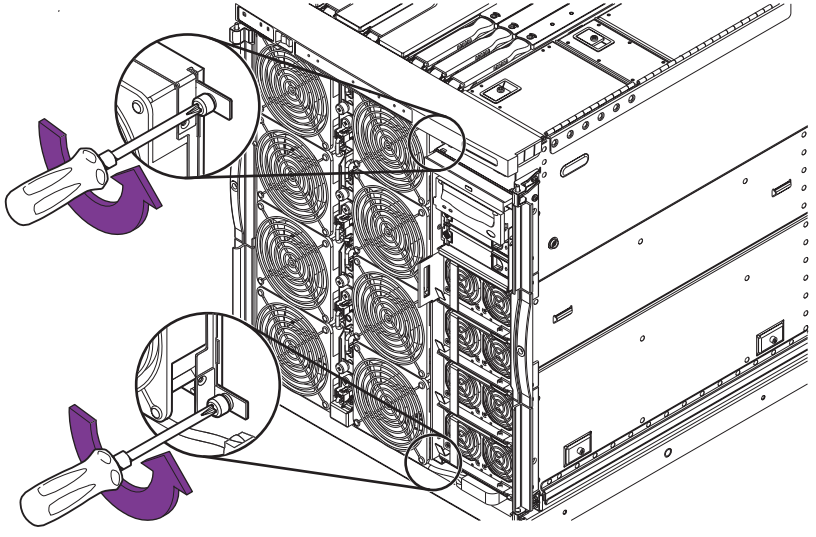


FIGURE 5-5 Loosening the Fan Tray Retaining Screws

7. **Pull the tray slightly to the right to disengage the mounting lugs.**
   Refer to FIGURE 5-6.

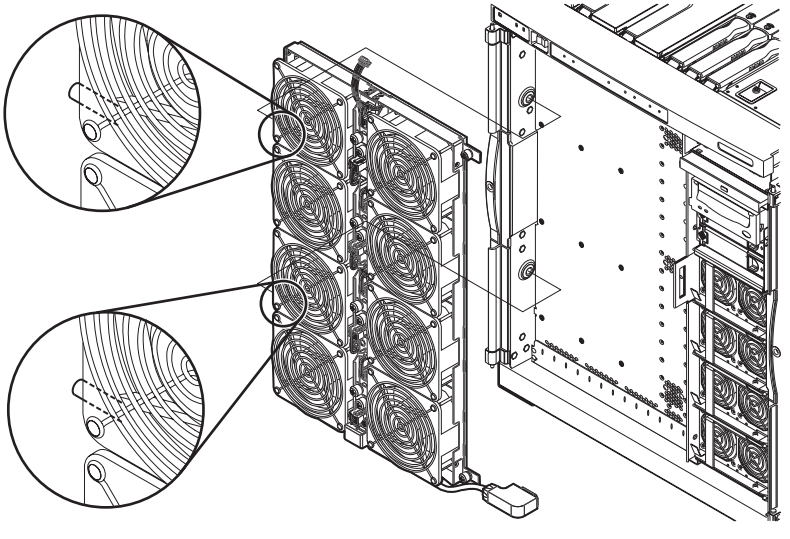


FIGURE 5-6 Removing the Fan Tray

8. **Remove the tray and place it on an ESD mat.**

5.2.2 To Install the Fan Tray

1. **Open the front doors of the system.**
2. **Attach the wrist strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5.
3. **Orient the tray so that the mounting lugs align with the cutouts in the system chassis on the left-hand side.**
4. **Gently push the tray into place and secure it by tightening the two captive screws, one at the top and one at the bottom right-hand side.**
5. **Plug in the fan tray power connector and the system indicator board connector.**

   Refer to Section 10.2, “Installing the System Indicator Board” on page 10-4.
6. **Replace the system indicator board connector retaining clip.**
7. **Remove the wrist strap.**
8. **Close the front doors of the system.**

5.3 IB Fans

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

Caution – This procedure requires the system to be extended out of the rack on its slides. Before attempting this procedure you must deploy rack stabilization devices, if fitted.

5.3.1 To Remove an IB Fan

1. **Deploy the rack stabilization device, if fitted.**
2. **Extend the system from the rack.**

   Loosen the captive screws securing the system to the rack and gently pull it out on its slides.

3. **Attach the wrist strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5.

4. **Open the IB fan cover.**

   Loosen the latch retaining screw, unlatch the cover and open it. Refer to FIGURE 5-7.

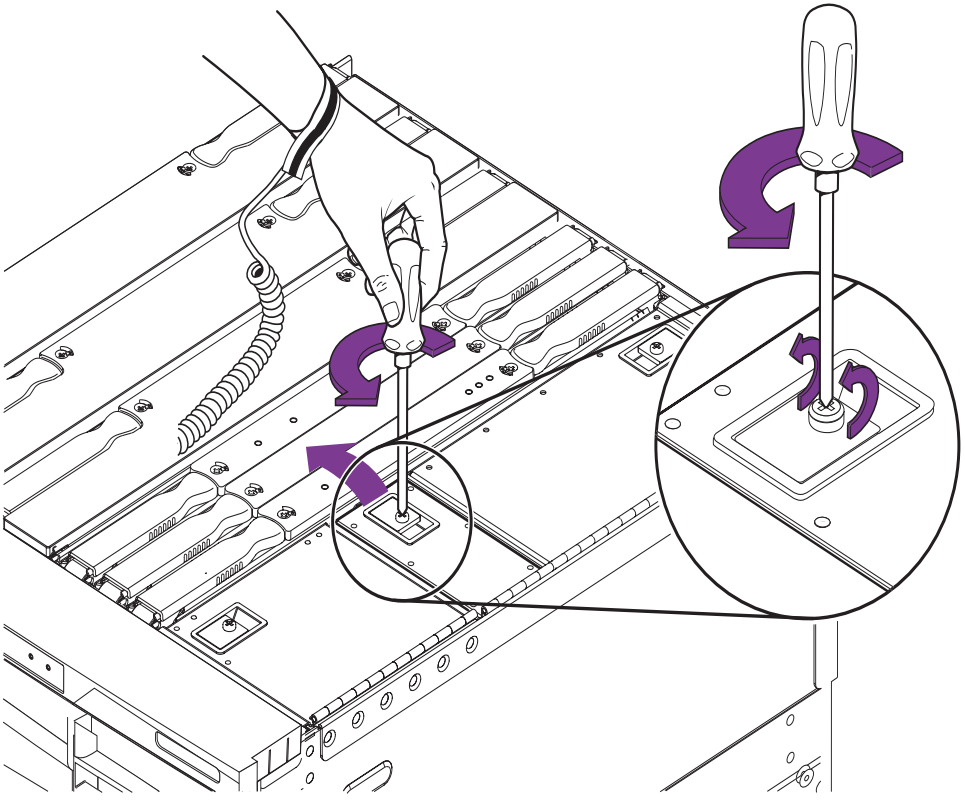


FIGURE 5-7 Opening the IB Fan Cover

5. **Identify the fan to be removed and unplug its power connector.**

Refer to FIGURE 1-7 and FIGURE 5-8.

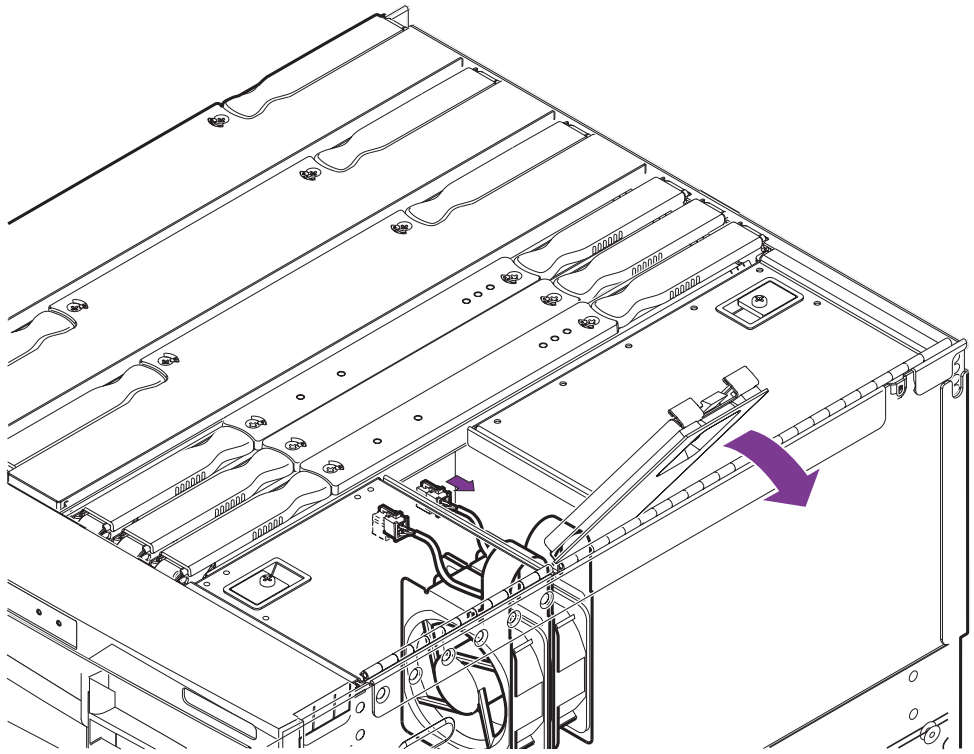


FIGURE 5-8 Identifying the Fan Connector

Caution – Wait at least ten seconds before removing the fan to allow it to stop rotating.

Caution – The remaining fan will still be rotating. Take care not to touch any part of it as there are no finger guards.

6. **Use the metal loop to lift the fan out of the chassis.**

   Refer to FIGURE 5-9.

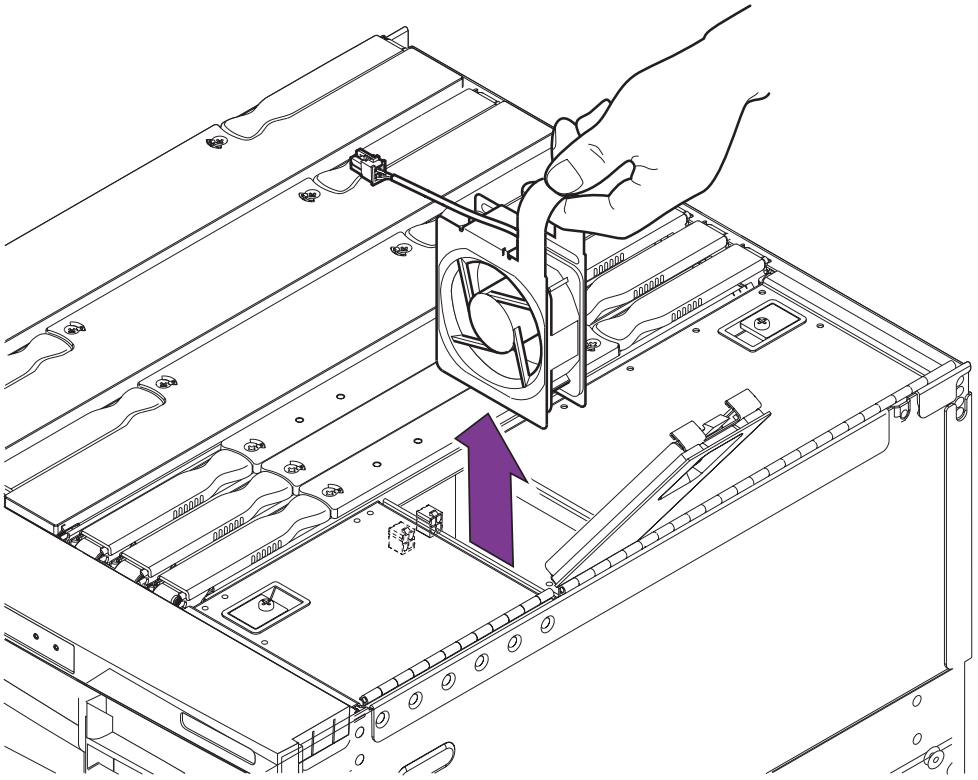


FIGURE 5-9 Removing an IB_SSC Fan

5.3.2 To Install an IB Fan

1. **Deploy the rack stabilization device, if fitted.**

2. **Extend the system from the rack.**

   Loosen the captive screws securing the system to the rack and gently pull it out on its slides.

3. **Attach the wrist strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5.

4. **Open the IB fan cover.**

   Loosen the latch retaining screw, unlatch the cover and open it. Refer to FIGURE 5-7.

5. **Use the metal loop to lower the fan into the chassis.**
6. **Plug in the fan's power connector.**

Caution – If the system is powered on, the fan will start as soon as the connector is inserted.

7. **Close and latch the fan cover.**
8. **Remove the wrist strap.**
9. **Slide the system back into the chassis and secure it.**
10. **Retract the rack stabilization device, if used.**

CHAPTER 6

Power Subsystem

This chapter described how to remove and install the various parts of the power subsystems. It contains the following sections:

A power supply can be replaced without powering down the system.

6.1 Power Supplies

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

Note – A minimum of two power supplies are required to be powered and working normally in order for the system to function correctly.

6.1.1 Removing a Power Supply

1. **Open the right-hand front door of the system.**
2. **Attach the wrist strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system. Place a grounded ESD mat close to the system.

3. **Identify the power supply to be removed.**

   Refer to FIGURE 1-9.

4. **Push in the metal spring on the left of the power supply, pull open the ejector lever and pull the power supply from the system.**

   Refer to FIGURE 6-1 and FIGURE 6-2.

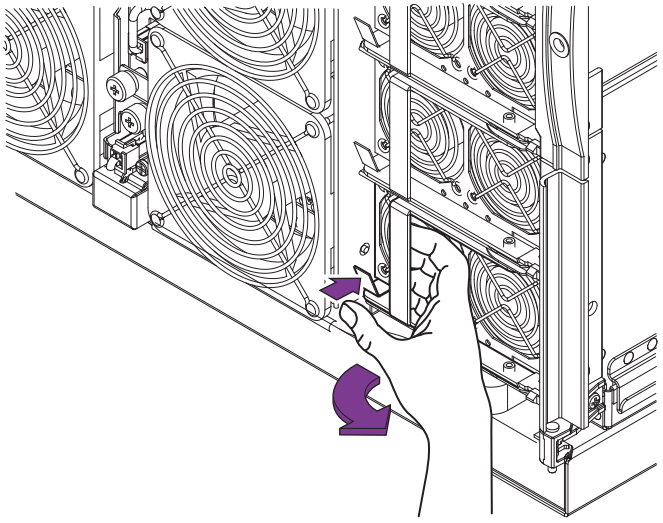


FIGURE 6-1 Unlatching a Power Supply

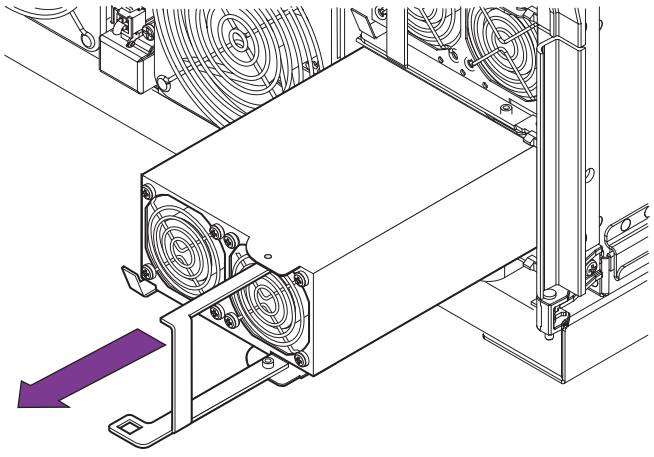


FIGURE 6-2 Removing the Power Supply

5. **Place it on an ESD mat.**

6.1.2 Installing a Power Supply

1. **Open the right-hand front door of the system.**
2. **Attach the wrist strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system.
3. **Ensure the ejector lever is extended fully from the power supply.**
4. **Push the power supply fully into its slot and close the ejector lever.**

   Ensure the latch has clicked home fully.
5. **Close the front door.**
6. **Remove the wrist strap.**

6.2 Power Inlet Box

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

6.2.1 Removing the Power Inlet Box

1. **Power down the system and remove the inlet power connector(s).**

   Refer to Section 3.3, “Powering Off” on page 3-4.
2. **Attach the wrist strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system. Place a grounded ESD mat close to the system.
3. **Remove the four Phillips #2 screws retaining the inlet box.**

   Refer to FIGURE 6-3.

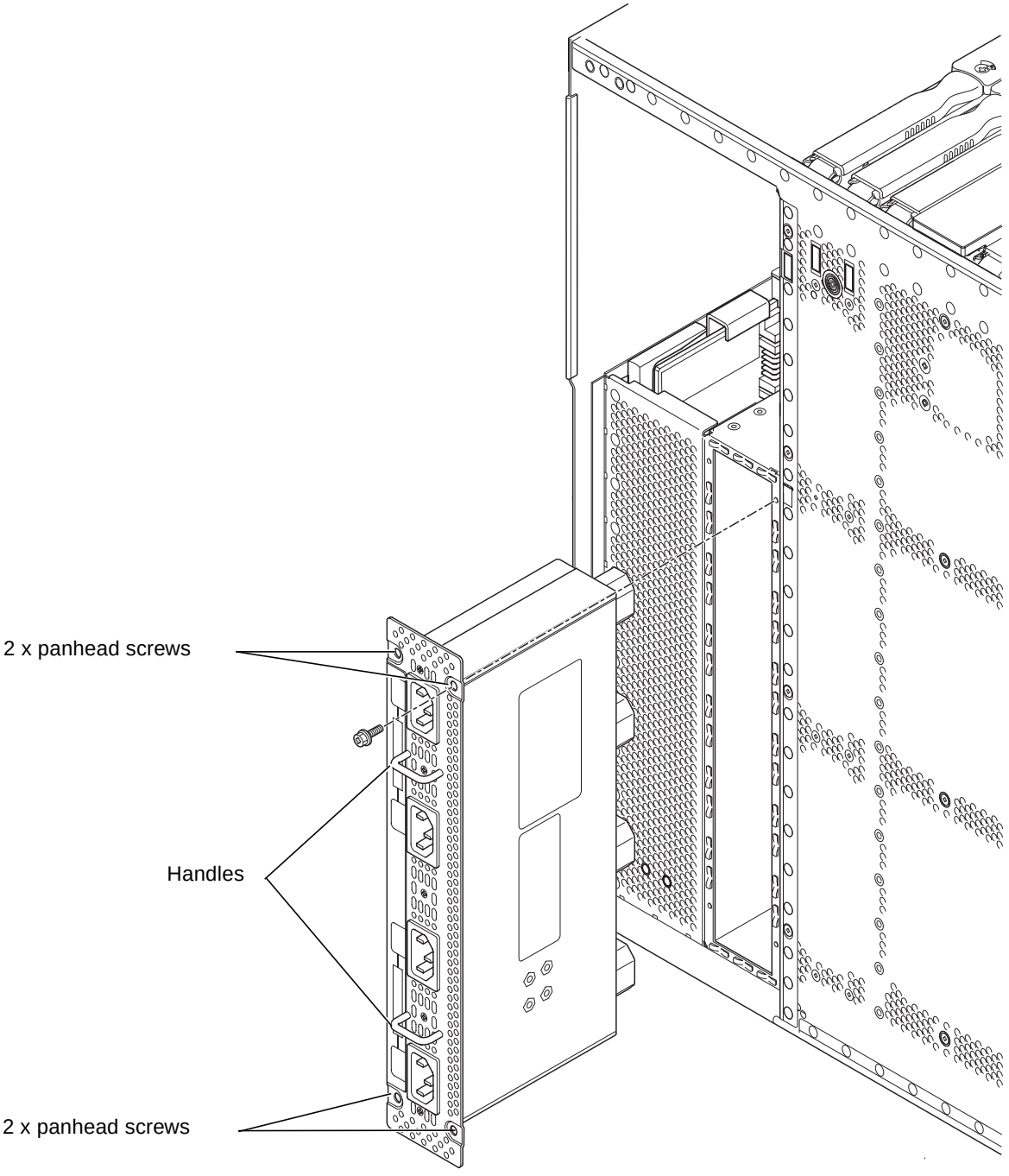


FIGURE 6-3 Removing the Power Inlet Box

4. **Withdraw the inlet box using the two handles and place it on an ESD mat.**

6.2.2 Installing the Power Inlet Box

1. **Insert the power inlet box into the rear of the system.**
2. **Secure the box using the the four countersunk Phillips #2 screws.**
3. **Insert the power inlet connectors.**
4. **Detach the wrist strap.**
5. **Power on the system.**

6.3 Power Distribution Board

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

Caution – This procedure requires the system to be extended out of the rack on its slides. Before attempting this procedure you must deploy rack stabilization devices, if fitted.

6.3.1 Removing the Power Distribution Board

1. **Power off the system and remove the input power connector(s).**

   Refer to Section 3.3, “Powering Off” on page 3-4.
2. **Extend and lock the rack stabiliser feet (if fitted).**
3. **Slide the system out of the rack.**

   Loosen the captive screws securing the system to the rack and gently pull it out on its slides.
4. **Open the right-hand front door.**

5. **Attach the wrist strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system. Place a grounded ESD mat close to the system.

6. **Remove the IB_SSC assembly.**

   Refer to Section 8.1.1, “Removing the IB_SSC Assembly” on page 8-1.

7. **Disengage all power supplies.**

   Refer to Section 6.1.1, “Removing a Power Supply” on page 6-1. There is no need to completely withdraw them from the system.

8. **Raise the power distribution board ejector lever (colored purple) until it is vertical.**

   Refer to FIGURE 6-4.

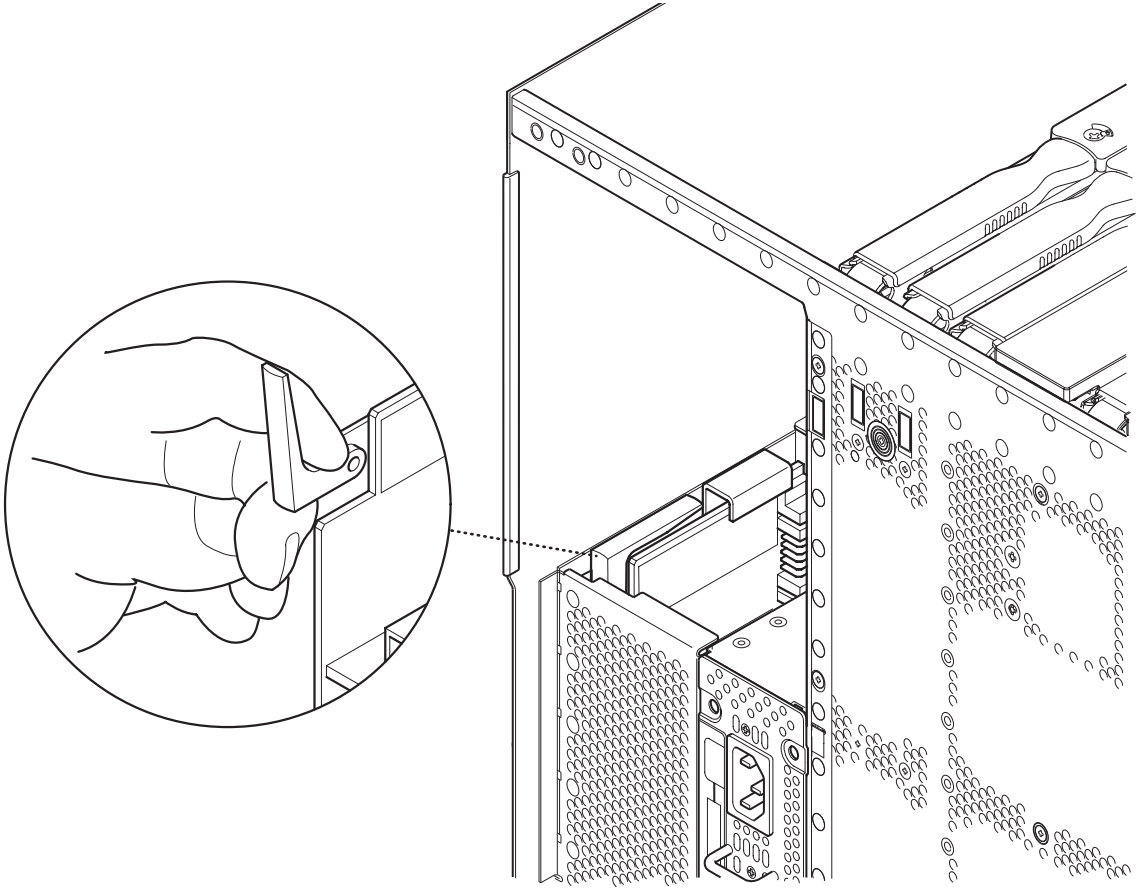


FIGURE 6-4 Disengaging the PDB Ejector Lever

9. **Use the metal handle to carefully pull the board upwards and out of the system.**
   Refer to FIGURE 6-5.

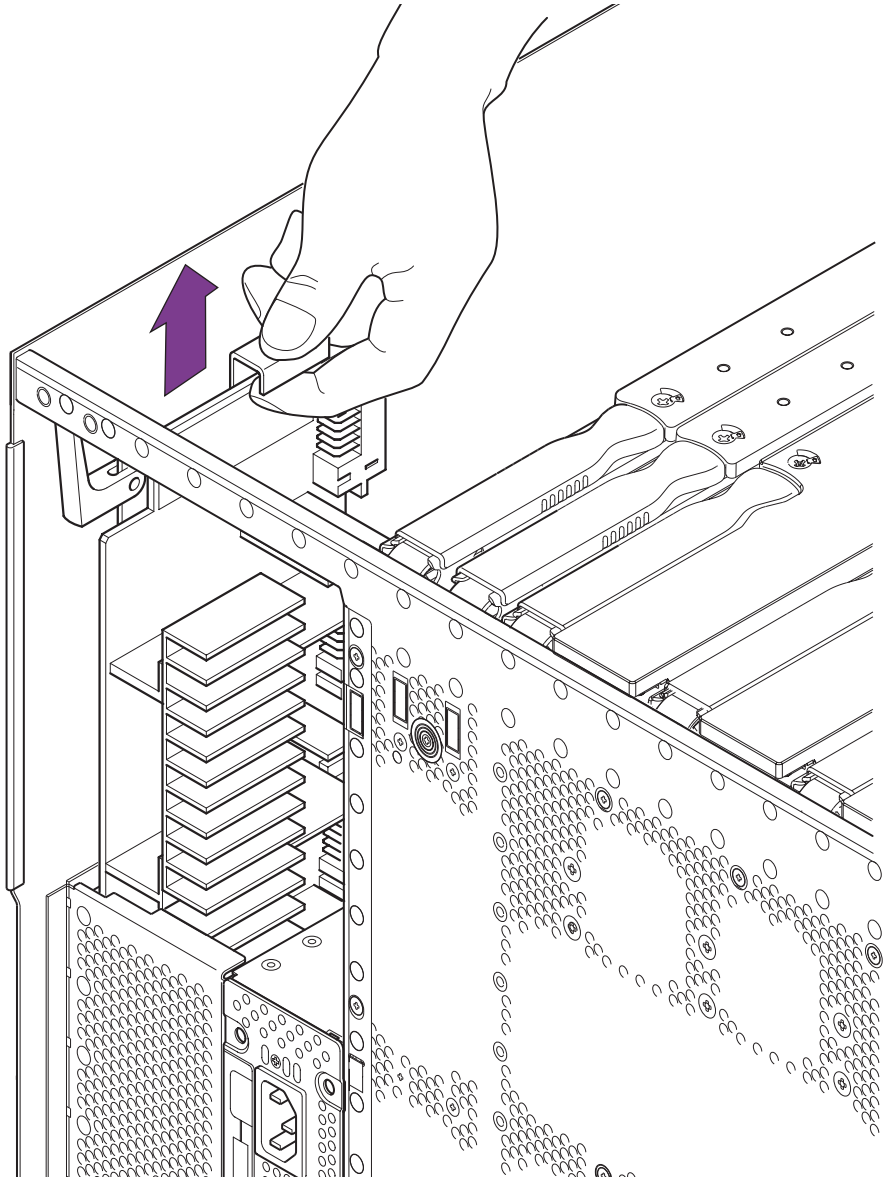


FIGURE 6-5 Removing the PDB

10. **Place the board on an ESD mat.**

6.3.2 Installing the Power Distribution Board

1.Attach the wrist strap.

Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system. Place a grounded ESD mat close to the system.

2. Locate the power distribution board into the card guides and gently slide it down to engage with the baseplane.

Refer to FIGURE 6-6.

3. Press down firmly to ensure the connector at the base of the board is firmly mated with the receptacle on the baseplane.

4. Ensure the purple ejector lever is horizontal.

5. Re-engage the power supplies.

6. Install the IB_SSC assembly.

Refer to Section 8.1.2, “Installing the IB_SSC Assembly” on page 8-4.

7. Detach the wrist strap.

8. Attach the inlet power cords.

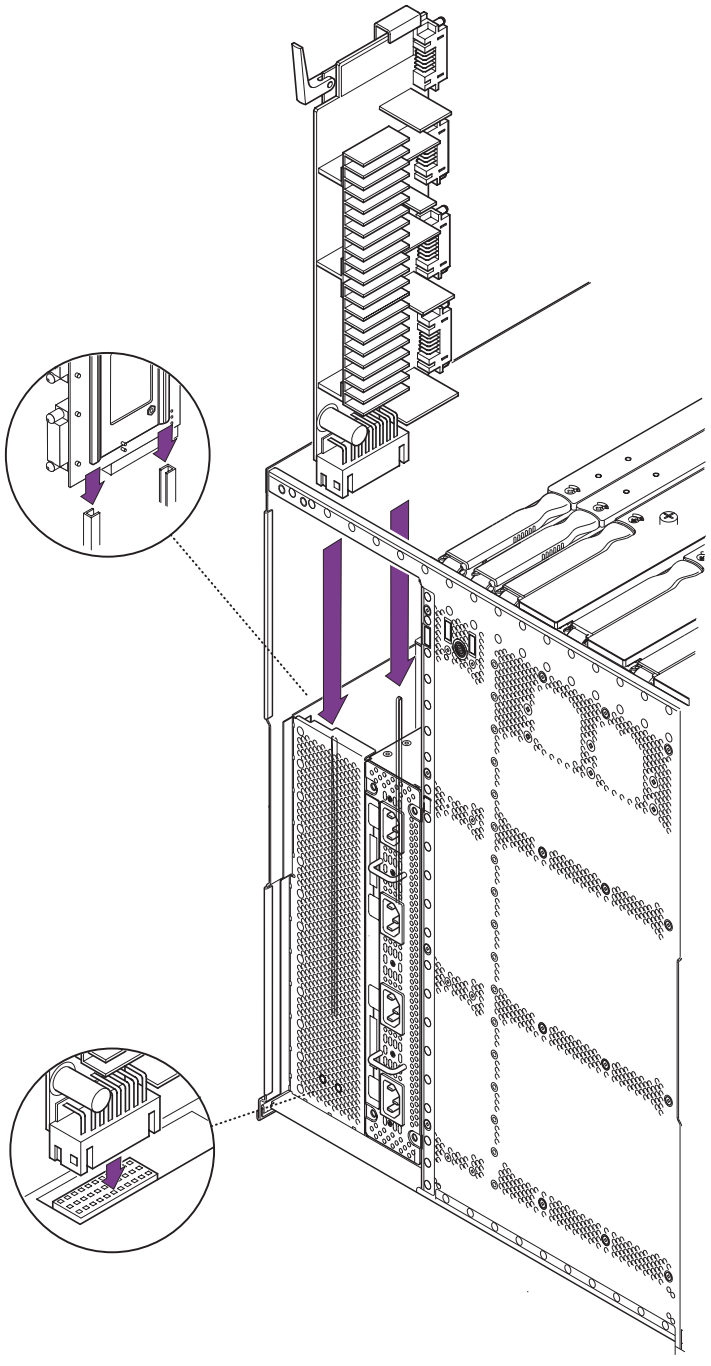


FIGURE 6-6 Inserting the PDB

CHAPTER 7

CPU / Memory boards

This chapter contains the following sections:

Note – If the system is powered on, before you begin this procedure, make sure that the fan tray is installed in the system and operating normally. The fan tray cools the CPU / Memory boards.

Note – Sun Fire V1280 CPU / Memory board field-replaceable unit (FRU) is for maintenance use only. FRUs must not be used to upgrade CPU performance in systems. Usage as such can violate U.S. export regulations.

Caution – This procedure requires the system to be extended out of the rack on its slides. Before attempting this procedure you must deploy rack stabilization devices, if fitted.

7.1 Filler Boards

In order to prevent the system from overheating when you permanently remove a CPU / Memory board from a system, install a filler board.

7.2 CPU / Memory Boards

All systems support the following:

- Four CPU processors with each processor supporting two DIMM (dual inline memory module) banks of four DIMMs per bank
- Eight Ecache modules (two per CPU processor)
- Up to 8 Gbytes of memory per CPU processor
- Up to 32 DIMMs

On the CPU / Memory board, the memory controller is integrated in the CPU processor. The CPU / Memory board has a metal cover that covers the CPU processors and Ecache.

There are three LEDs on the CPU / Memory board. TABLE 7-1 notes the LED functions.

TABLE 7-1 CPU / Memory board LED Functions

LED	On	Off
Activated LED (green)	Device is activated.	Device is deactivated
Fault LED (amber)	Internal fault	No internal fault
OK to remove (amber)	Assembly can be removed	Assembly cannot be removed

FIGURE 7-1 illustrates the CPU / Memory board LEDs and indications.

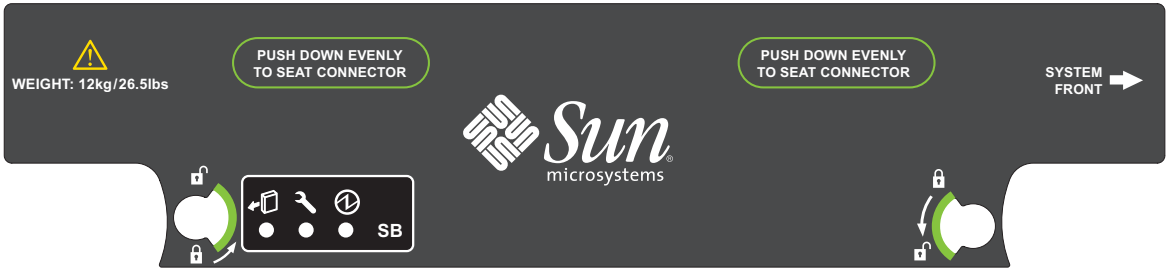


FIGURE 7-1 CPU / Memory board Labels and Indications

7.2.1 Removing a CPU/Memory Board

Caution – The CPU/Memory board is heavy and weighs approximately 12 kg (26.5 pounds). Take care when removing the board from the system.

1. **Ensure that any resources in use by the CPU/Memory board to be replaced have been unconfigured.**

2. **Detach and power off the board by using the `cfgadm -c disconnect` command.**

```
# cfgadm -c disconnect ap_id
```

   where *ap_id* is one of the following: `N0.SB0`, `N0.SB2` or `N0.SB4`.

   The OK to Remove LED should be lit.

3. **Extend and lock the rack stabiliser feet (if fitted).**

4. **Slide the system out of the rack.**

   Loosen the captive screws securing the system to the rack and gently pull it out on its slides.

5. **Be sure that you have a filler board (if necessary) or replacement board ready.**

   Refer to Section 7.1, “Filler Boards” on page 7-1.

6. **Attach a wrist strap or foot strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system. Place a grounded ESD mat close to the system.

7. **Unlock the ejector levers on the CPU/Memory board with a Phillips #2 screwdriver (**FIGURE 7-2**).**

   The ejectors will pop out slightly.

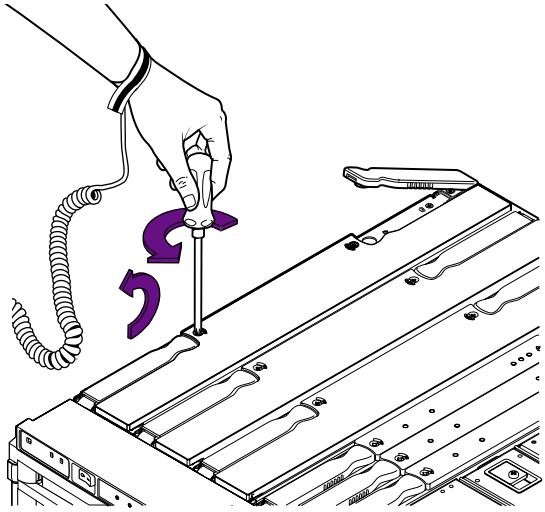


FIGURE 7-2 Unlocking the CPU/Memory board Ejector Levers

8. **Raise the ejector levers simultaneously until they are 90 degrees straight out from the board (**FIGURE 7-3**).**

   This action unseats the board from the baseplane connector.

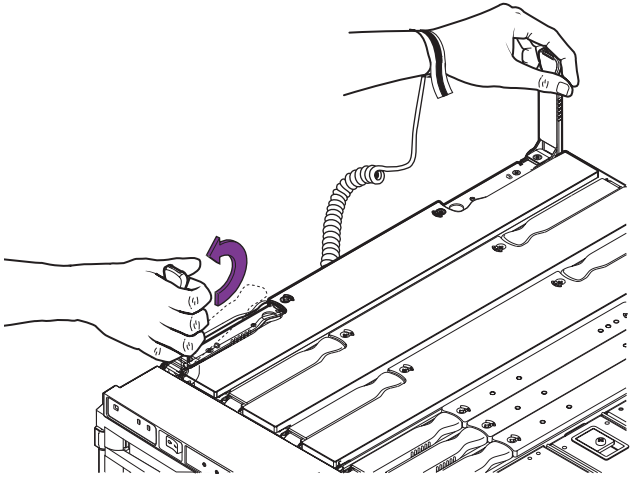


FIGURE 7-3 Raising the CPU/Memory board Ejector Levers

9. Raise the CPU/Memory board by grasping the ejector levers and pulling upwards.

The anti-gravity guides allow you to raise the board halfway and then remove both hands without the board sliding down again, in order for you to change your grip (FIGURE 7-4).

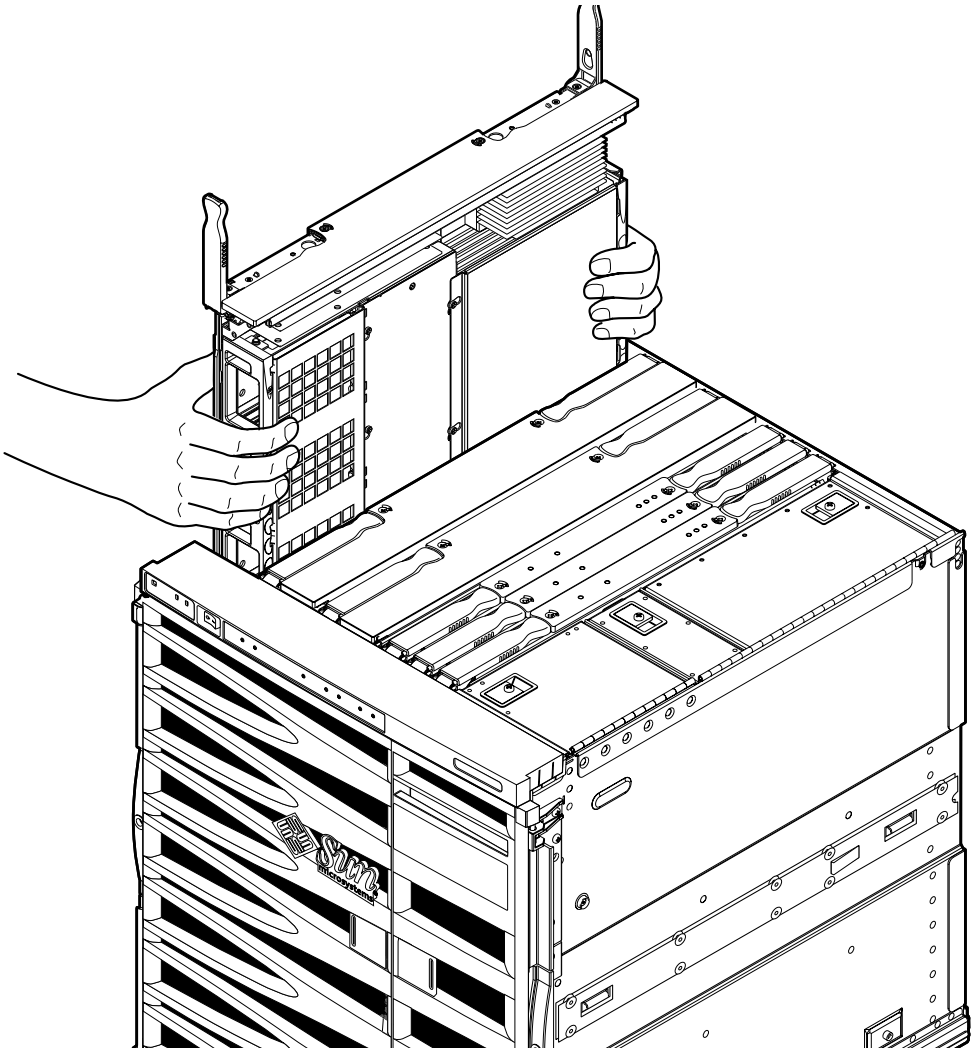


FIGURE 7-4 Raising a CPU / Memory board Halfway Utilizing the Anti-Gravity Guides

10. Place the board on a grounded ESD mat.

11. **Remove the DIMMs and install them in the replacement board (if one is to be fitted).**

    Refer to Section 7.3.2, “Removing DIMMs” on page 7-9.

Caution – Install a filler board in the empty slot if no replacement board is going to be installed to prevent overheating when the system is powered back on. Refer to Section 7.1, “Filler Boards” on page 7-1.

7.2.2 Installing a CPU/Memory Board

1. **Attach a wrist strap or foot strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system.

2. **Install DIMMs into the module, if rquired.**

   Refer to Section 7.3.3, “Installing DIMMs” on page 7-10.

3. **Remove the CPU/Memory board filler board, if fitted.**

4. **Make sure that the ejector levers of the CPU/Memory board are in the open position.**

   They should be 90 degrees straight out from the board (FIGURE 7-2).

Caution – DO NOT FORCE any board into a slot; it can cause damage to the board and system. The board should insert and seat smoothly. If it binds, remove the board and inspect the card cage slot for any obvious obstructions. Also inspect both the board and the baseplane for bent pins or other damage.

5. **Grasping the green fingerhold panels, gently insert the CPU/Memory board into the grooves into the proper slot.**

   You can release the panels when the board is inserted halfway in order to change your grip. Refer to (FIGURE 7-4).

6. **When the board is nearly fully inserted it will drop free on to the ejectors.**

   This is correct.

7. **Simultaneously lower both ejectors until they are in the closed position (flush with the board).**

   When properly installed, the ejectors will lock automatically.

8. **Power on, test, and configure the board using the** `cfgadm -c configure` **command**:

```
# cfgadm -c configure ap_id
```

where *ap_id* is one of the following: `N0.SB0`, `N0.SB2` or `N0.SB4`.

7.3 DIMMS

The CPU/Memory board has 32 DIMM sockets, which are divided into eight banks of four DIMMs per bank. Each CPU processor has two corresponding DIMM banks. It is possible that a CPU processor does not have any DIMMs installed in its corresponding DIMM bank. However, a populated DIMM bank must have a corresponding CPU processor installed.

Three types of DIMM can be used in the DIMM banks:

- 256 Mbytes
- 512 Mbytes
- 1 Gbyte

FIGURE 7-5 illustrates the DIMM numbers for the eight DIMM banks.

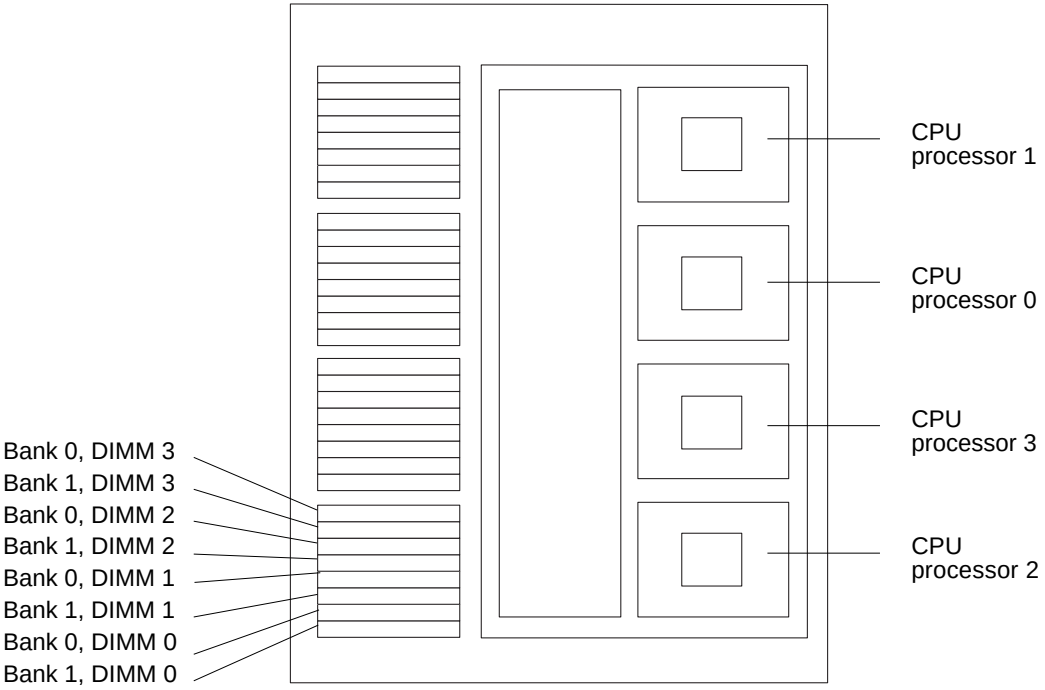


FIGURE 7-5 DIMM Slot Numbers

The DIMM number and bank number are repeated in the same order as CPU processor 2 for CPU processor 3, CPU processor 0, and CPU processor 1. DIMM number 3, bank 0 is the first DIMM, and DIMM number 3, bank 1 is the second DIMM in each DIMM bank. The CPU processor number is noted on the metal cover.

7.3.1 DIMM Bank Configuration Guidelines

Follow these DIMM configuration guidelines:

- Each DIMM bank must be fully populated with the same capacity DIMM.
- Install the larger capacity DIMMs into banks before installing the smaller capacity DIMMs into banks.
- The minimum number of DIMMs you can install per CPU processor is four DIMMs or one bank.
- If the number of CPU processors on each CPU/Memory board are the same, place DIMM banks on CPU/Memory boards that have fewer populated DIMM banks before placing DIMMs on CPU/Memory boards that already have more populated DIMM banks.

- If some CPU/Memory boards have more CPU processors than others, place DIMMs in DIMM banks on the board with the most CPU processors. There will be CPU processors without corresponding DIMMs on other boards.

7.3.2 Removing DIMMs

Caution – The system is sensitive to static electricity. Make sure you are wearing a grounded wrist strap when handling system components. Always place components on a grounded ESD mat close to the system.

1. **Remove the applicable CPU/Memory board.**

   See Section 7.2.1, “Removing a CPU/Memory Board” on page 7-3.”

2. **Place the CPU/Memory board on the ESD mat on a work surface.**

3. **Remove the four screws retaining the DIMM cover and remove the cover.**

   Refer to FIGURE 7-6.

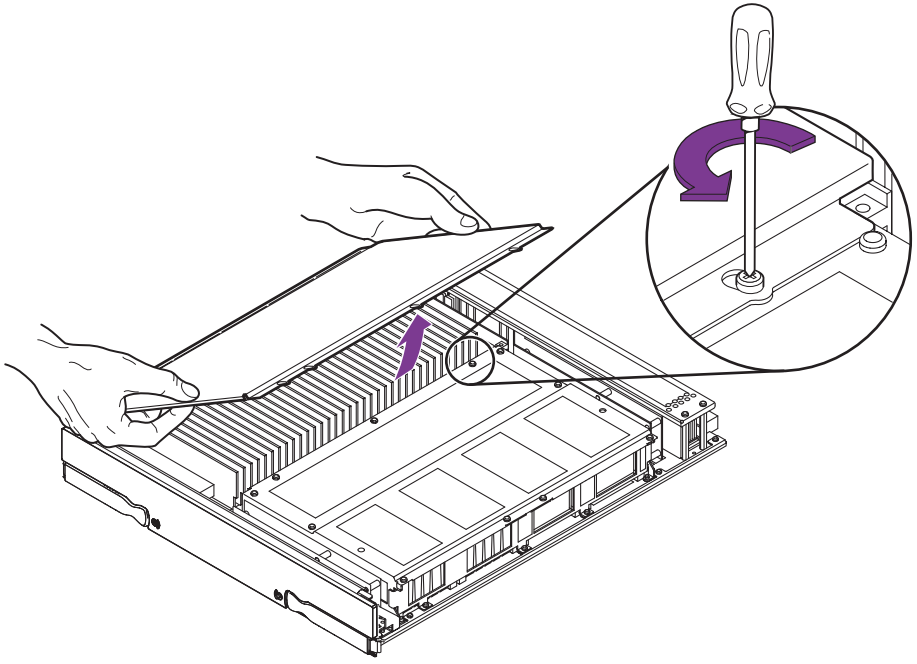


FIGURE 7-6 Removing the DIMM Cover

4. **Locate the slot for the DIMM you need to replace.**

5. **Eject the faulty DIMM by pressing down on the ejection levers on both sides of the DIMM connector (**FIGURE 7-7**).**

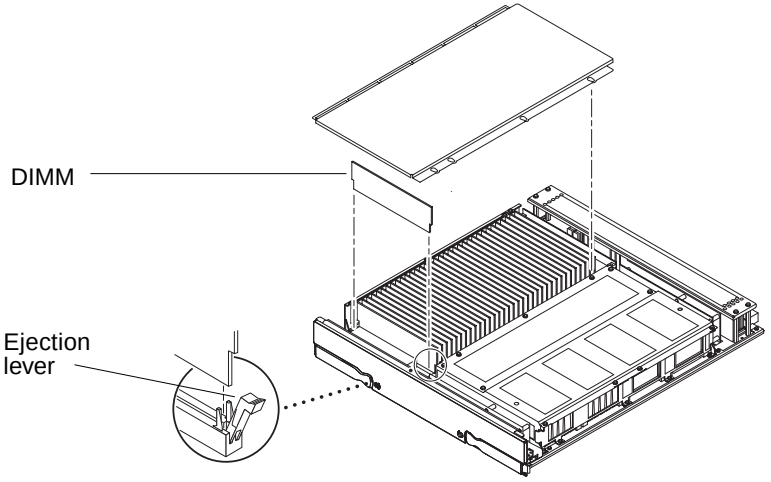


FIGURE 7-7 Removing a DIMM

6. **Holding the DIMM by its edges, remove it from the slot and place it on an antistatic surface.**

7. **Replace the DIMM cover and secure it using the four screws.**

7.3.3 Installing DIMMs

Install one bank completely on each board before installing the remaining banks on any board.

Note – All banks must have the same size DIMMs. However, DIMMs from different manufacturers are interchangeable in a single bank if the DIMMs all have the same capacity and speed. Sort the DIMMs into banks using the same size DIMMs.

Caution – The system and DIMMs are sensitive to static electricity. To prevent damage to the DIMMs, make sure you are wearing a grounded wrist strap when handling them. Always place components on a grounded ESD mat close to the system.

---

1. **Remove the applicable CPU/Memory board.**

   See Section 7.2.1, “Removing a CPU/Memory Board” on page 7-3.”

2. **Place the CPU/Memory board on an ESD mat on a work surface.**

3. **Remove the four screws retaining the DIMM cover and remove the cover.**

   Refer to FIGURE 7-6.

4. **Carefully remove the new DIMM from its protective packaging and place it on an antistatic surface.**

   The bag that the DIMM is packed in makes a good antistatic surface.

5. **Press down on the ejector levers at both ends of the DIMM connector slot that will receive the new DIMM.**

   The connector slot will not accept the DIMM unless the levers are in the insert (open) position.

6. **Align the short-side key on the DIMM and the long-side key on the DIMM with the short side and long side of the DIMM connector.**

Note – If you are installing four DIMMs, insert the DIMMs into the same bank.

---

7. **Place your thumbs on the top edge of the DIMM, and push the DIMM firmly into its connector (**FIGURE 7-8**).**

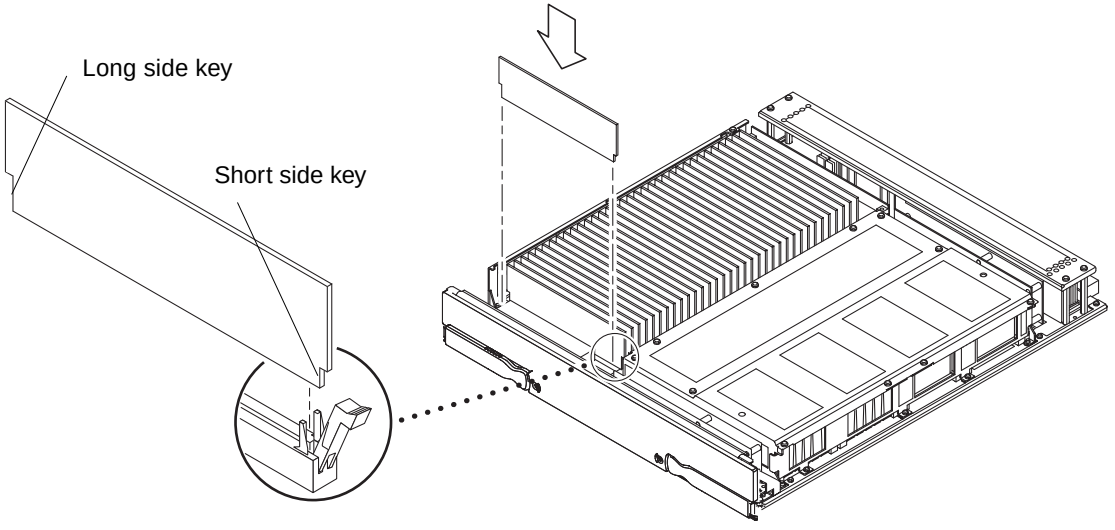


FIGURE 7-8 Installing a DIMM

8. **Press down firmly on the entire edge of the DIMM.**

   When installed correctly, the ejector levers will be in the upright position.

9. **Continue installing DIMMs in the same manner.**

10. **Replace the DIMM cover and secure it using the four screws.**

11. **Reinstall the CPU/Memory board and detach the wrist strap.**

    See Section 7.2.2, “Installing a CPU/Memory Board” on page 7-6.

CHAPTER 8

IB_SSC Assembly

Caution – This procedure requires the system to be extended out of the rack on its slides. Before attempting this procedure you must deploy rack stabilization devices, if fitted.

8.1 IB_SSC Assembly

8.1.1 Removing the IB_SSC Assembly

Caution – The IB_SSC assembly is heavy and weighs approximately 11 kg (24 pounds); it is also an awkward shape to handle. Take care when removing the board from the system.

1. **Power off the system and remove the input power connector(s).**

   Refer to Section 3.3, “Powering Off” on page 3-4.

2. **Extend and lock the rack stabiliser feet (if fitted).**

3. **Remove all connectors from the rear of the system.**

4. **Slide the system out of the rack.**

   Loosen the captive screws securing the system to the rack and gently pull it out on its slides.

5. **Attach a wrist strap or foot strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system. Place a grounded ESD mat close to the system.

6. **Open the removable media bay cover.**

   Refer to FIGURE 8-1.

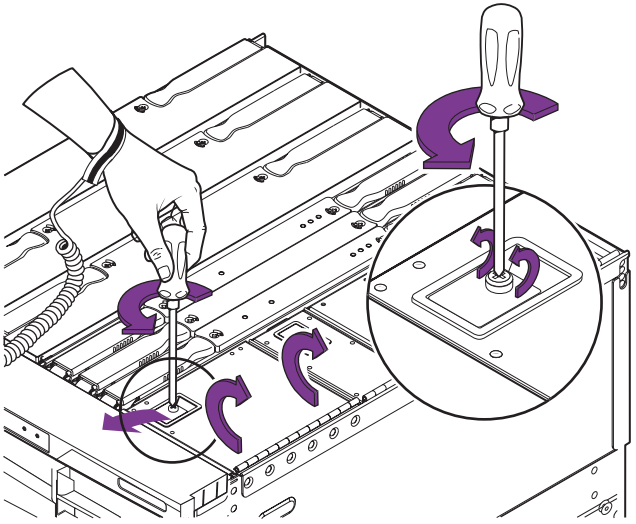


FIGURE 8-1 Opening the Media Bay Cover

7. **Disconnect the cables from the IB_SSC assembly to the removable media modules and secure them out of the way.**

   It will be necessary to remove the foam air filter covering the IB fan intake grille.

8. **Remove the PCI cards from the PCI bay.**

   Refer to Section 8.2.1, “Removing a PCI Card” on page 8-6.

9. **Unlock the ejector levers on the IB_SSC assembly with a Phillips #2 screwdriver (**FIGURE 8-2**).**

   The ejectors will pop out slightly.

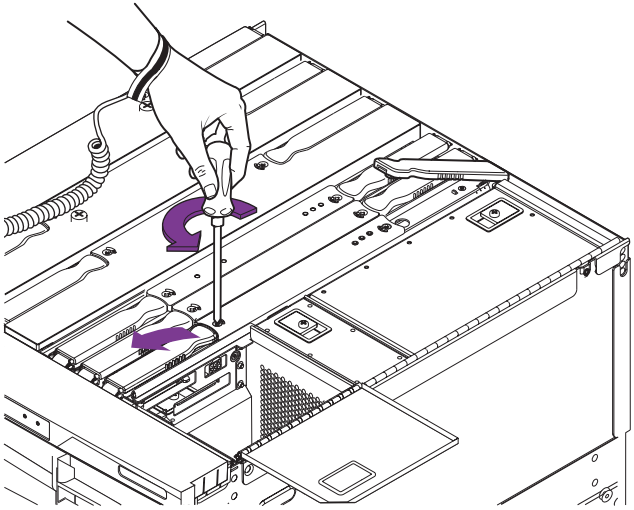


FIGURE 8-2 Unlocking the IB_SSC Assembly Ejector Levers

10. **Raise the ejector levers simultaneously until they are 90 degrees straight out from the board.**

    This action unseats the board from the connector.

11. **Raise the IB_SSC assembly.**

    The anti-gravity guides allow you to raise the board halfway and then remove both hands without the board sliding down again in order for you to change your grip (FIGURE 8-3).

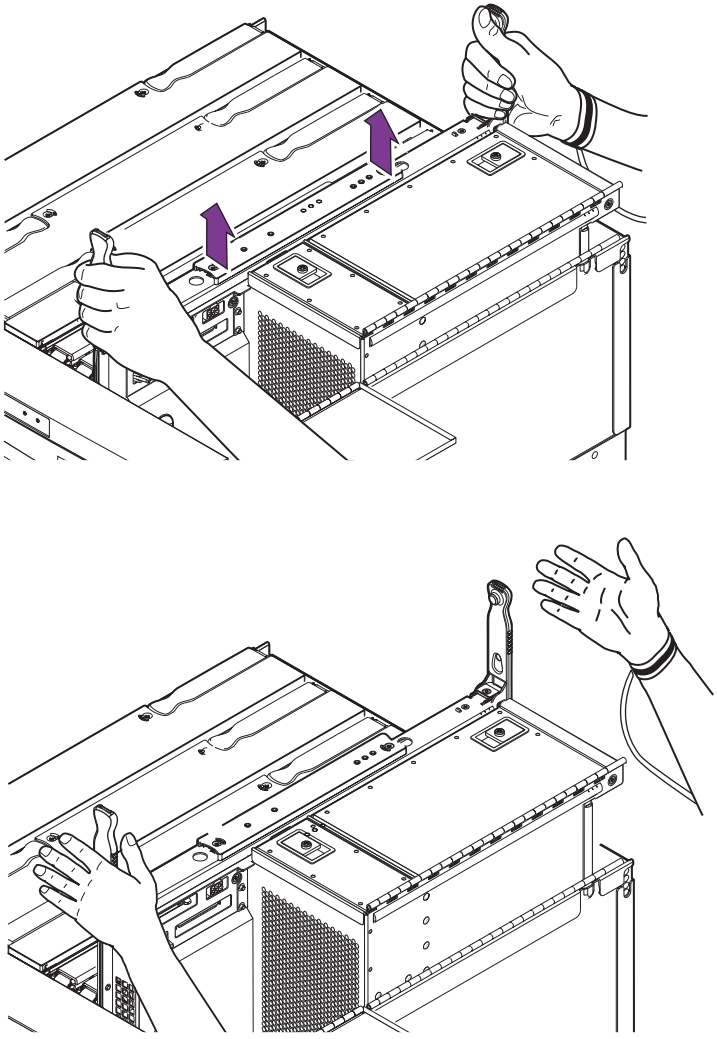


FIGURE 8-3 Raising a IB_SSC Assembly Halfway Utilizing the Anti-Gravity Guides

12. **Place the board on a grounded ESD mat.**

8.1.2 Installing the IB_SSC Assembly

1. **Attach a wrist strap or foot strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system.

2. **Ensure the removable media cables are safely out of the way.**

3. **Make sure that the ejector levers of the IB_SSC assembly are in the open position. They should be 90 degrees straight out from the board (**FIGURE 8-2**).**

Caution – DO NOT FORCE any board into a slot; it can cause damage to the board and system. The board should insert and seat smoothly. If it binds, remove the board and inspect the card cage slot for any obvious obstructions. Also inspect both the board and the baseplane for bent pins or other damage.

4. **Using the injector levers, gently insert the IB_SSC assembly into the grooves into the proper slot.**

   You can release the levers when the board is inserted halfway in order to change your grip. Refer to (FIGURE 8-3).

5. **When the board is nearly fully inserted it will drop free on to the ejectors.**

   This is correct.

6. **Simultaneously lower both ejectors until they are in the closed position (flush with the board).**

   When properly installed, the ejectors will lock automatically.

7. **Install the PCI cards.**

   Refer to Section 8.2.2, “Installing a PCI Card” on page 8-9.

8. **Reconnect the cables from the removable media modules to the IB_SSC assembly.**

   If necessary, replace the foam air filter against the IB fan air intake grille.

9. **Close the removable media bay and PCI bay covers.**

10. **Reconnect the cables to the rear of the system**

11. **Remove the antistatic wrist or foot strap.**

12. **Slide the system into the rack and secure it.**

13. **Complete the power-on steps.**

    Refer to Section 3.2, “Powering On” on page 3-2 for complete procedures for powering on the system.

8.2 PCI Cards

Caution – This procedure requires the system to be extended out of the rack on its slides. Before attempting this procedure you must deploy rack stabilization devices, if fitted.

8.2.1 Removing a PCI Card

Caution – If you remove a PCI card and are not going to replace it, you must fit a PCI card blanking panel in its place to maintain EMI integrity.

1. **Power off the system to standby.**

   Refer to Section 3.2, “Powering On” on page 3-2.

2. **Extend and lock the rack stabiliser feet (if fitted).**

3. **Slide the system out of the rack.**

   Loosen the captive screws securing the system to the rack and gently pull it out on its slides.

4. **Attach a wrist strap or foot strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system. Place a grounded ESD mat close to the system.

5. **Remove the appropriate connector(s) from the rear of the system.**

6. **Open the PCI bay cover.**

   Refer to FIGURE 8-4.

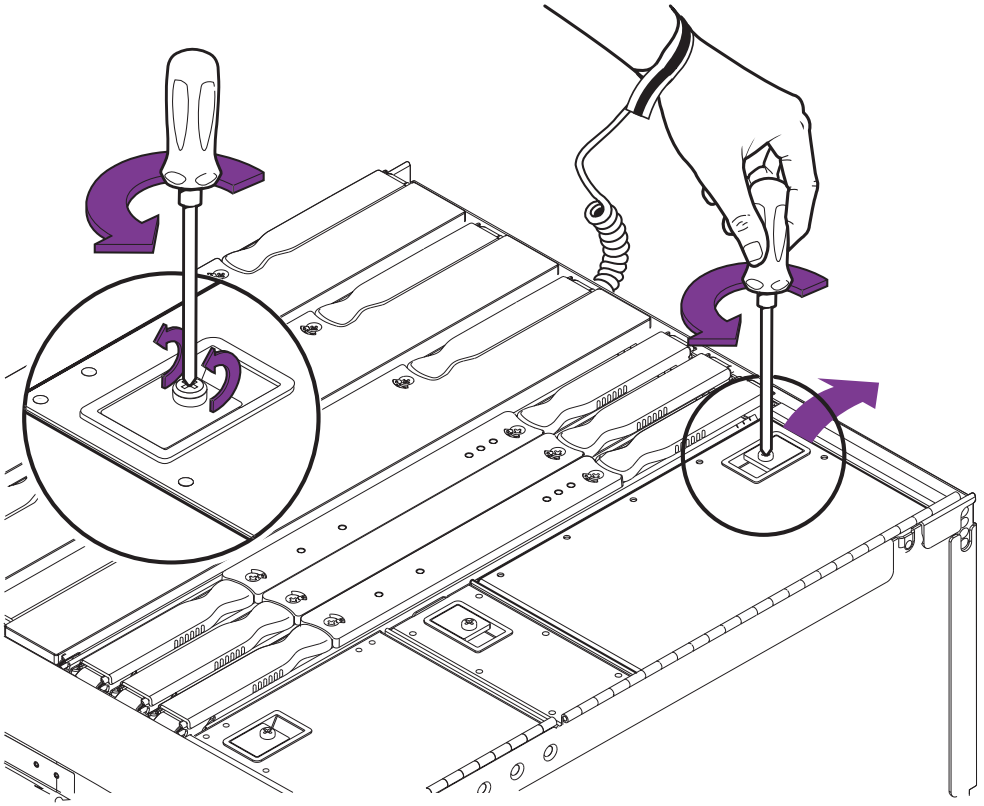


FIGURE 8-4 Opening the PCI Bay Cover

7. **Identify the card to be removed.**

8. **Unscrew the retaining screw, then gently pull the card upwards until it is free of the IB_SSC receptacle.**

   Refer to FIGURE 8-5 and FIGURE 8-6.

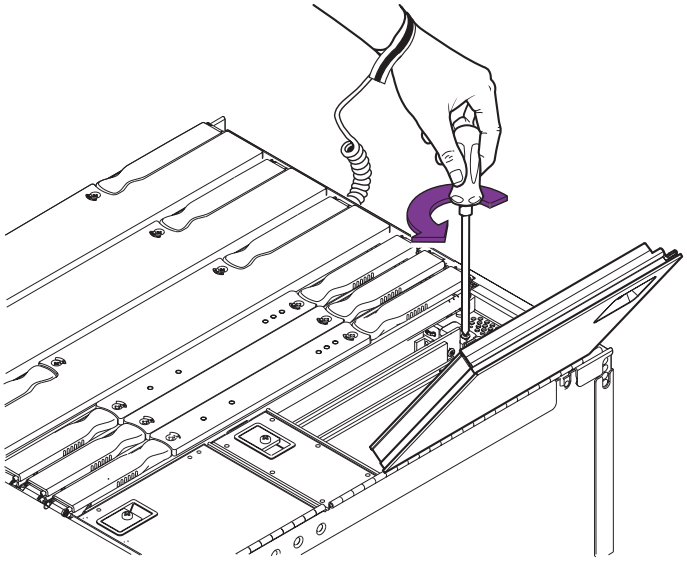


FIGURE 8-5 Removing the PCI Card Retaining Screw

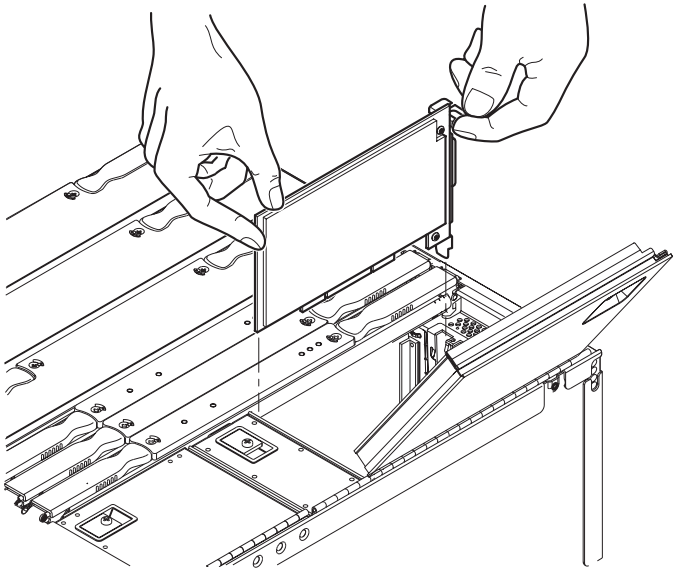


FIGURE 8-6 Removing a PCI Card

9. Place the card on a grounded ESD mat.

8.2.2 Installing a PCI Card

Caution – This procedure requires the system to be extended out of the rack on its slides. Before attempting this procedure you must deploy rack stabilization devices, if fitted.

1. **Power off the system to standby.**

   Refer to Section 3.3, “Powering Off” on page 3-4.

2. **Extend and lock the rack stabiliser feet (if fitted).**

3. **Slide the system out of the rack.**

   Loosen the captive screws securing the system to the rack and gently pull it out on its slides.

4. **Attach a wrist strap or foot strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system. Place a grounded ESD mat close to the system.

5. **Open the PCI bay cover.**

6. **Locate the connector into which the card is to be installed, then press the card gently into its receptacle in the IB_SSC until it is fully seated.**

7. **Secure the card with its retaining screw.**

8. **Close the PCI bay cover and secure it.**

9. **Plug the appropriate cable into the connector at the rear of the system.**

10. **Remove the antistatic wrist or foot strap.**

11. **Slide the system into the rack and secure it.**

12. **Complete the power-on steps.**

    Refer to Section 3.2, “Powering On” on page 3-2 for complete procedures for powering on the system.

CHAPTER 9

L2 Repeaters

Caution – This procedure requires the system to be extended out of the rack on its slides. Before attempting this procedure you must deploy rack stabilization devices, if fitted.

9.1 Replacing an L2 Repeater Board

1. **Power down the system to standby.**

   Refer to Section 3.3, “Powering Off” on page 3-4.

2. **Extend and lock the rack stabiliser feet (if fitted).**

3. **Slide the system out of the rack.**

   Loosen the captive screws securing the system to the rack and gently pull it out on its slides.

4. **Be sure that you have a replacement board ready.**

5. **Attach a wrist strap or foot strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system. Place a grounded ESD mat close to the system.

6. **Unlock the ejector levers with a Phillips #2 screwdriver (**FIGURE 9-1**).**

   The ejectors will pop out slightly.

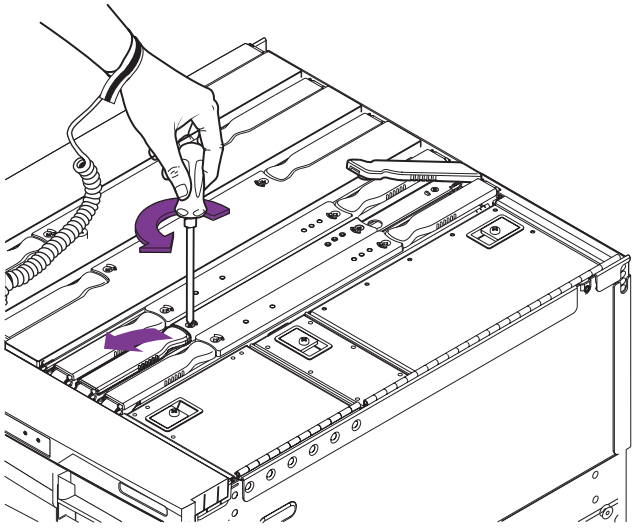


FIGURE 9-1 Unlocking the L2 Repeater Board Ejector Levers

7. **Raise the ejector levers simultaneously until they are 90 degrees straight out from the board.**

   This action unseats the board from the connector.

8. **Raise the L2 repeater board using the ejector levers.**

   The anti-gravity guides allow you to raise the board halfway and then remove both hands without the board sliding down again in order for you to change your grip (FIGURE 9-2).

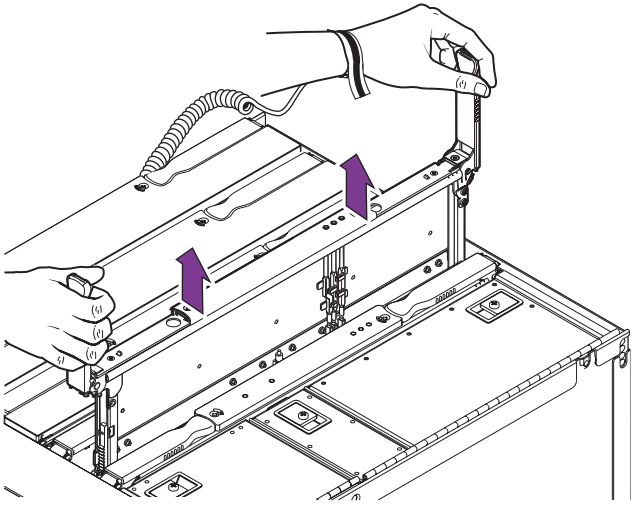


FIGURE 9-2 Raising an L2 Repeater Board

9. **Place the board on a grounded ESD mat.**

10. **Make sure that the ejector levers of the replacement L2 repeater board are in the open position.**

    They should be 90 degrees straight out from the board (FIGURE 9-1).

Caution – DO NOT FORCE any board into a slot; it can cause damage to the board and system. The board should insert and seat smoothly. If it binds, remove the board and inspect the card cage slot for any obvious obstructions. Also inspect both the board and the baseplane for bent pins or other damage.

11. **Using the injector levers, gently insert the L2 repeater board into the grooves into the proper slot.**

    You can release the levers when the board is inserted halfway in order to change your grip. Refer to (FIGURE 9-3).

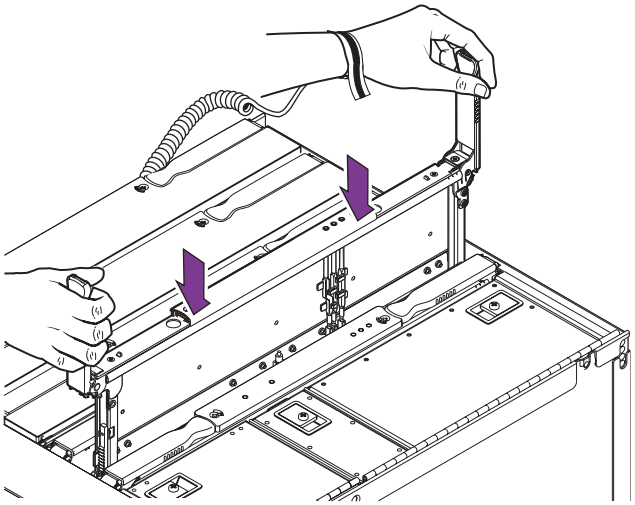


FIGURE 9-3 Inserting an L2 Repeater Board

12. **When the board is nearly fully inserted it will drop free on to the ejectors.**

    This is correct.

13. **Simultaneously lower both ejectors until they are in the closed position (flush with the board).**

    When properly installed, the ejectors will lock automatically.

14. **Complete the power-on steps.**

    Refer to Section 3.2, “Powering On” on page 3-2 for complete procedures for powering on the system.

CHAPTER **10**

System Indicator Board

This chapter describes how to remove and install the system indicator board, which contains the On/Standby switch and the various system indicator LEDs

The board can only be removed after powering off the system.

10.1 Removing the System Indicator Board

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Power off the system and remove the input power connector(s).**

   Refer to “Powering Off” on page 3-4.

2. **Open the front doors of the system.**

3. **Attach the wrist strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5.

4. **Press in the front of the system indicator board housing and unclip it from its mounting.**

   Refer to FIGURE 10-1.

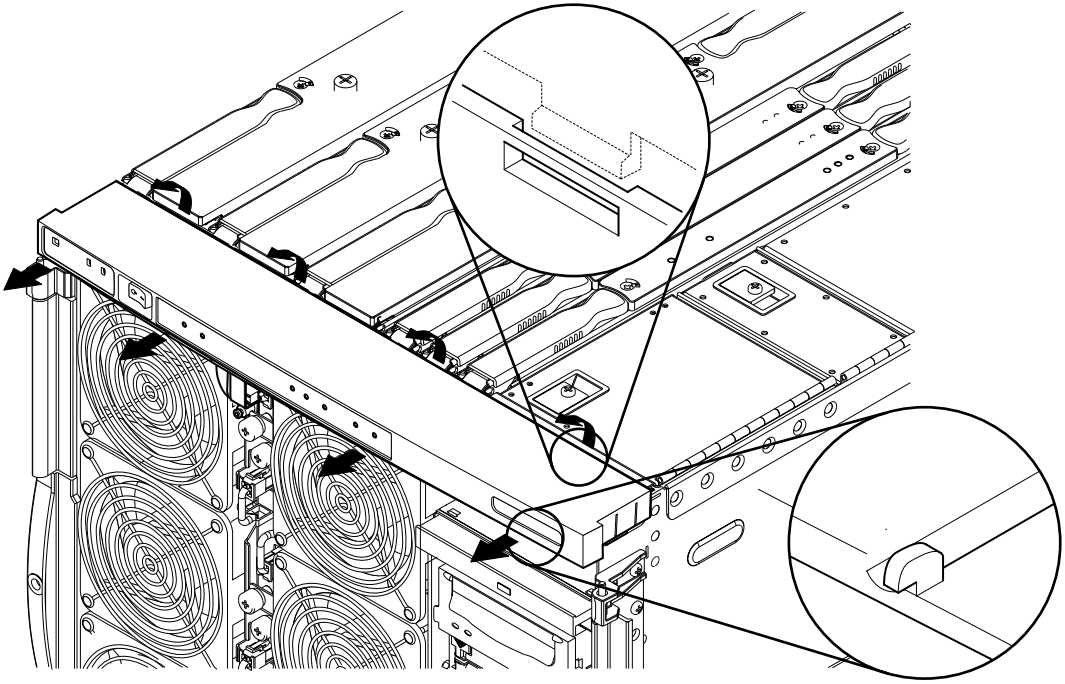


FIGURE 10-1 Removing the System Indicator Board Cover

5. **Remove the clip on the fan tray retaining the system indicator board connector and remove the connector.**

   Refer to FIGURE 10-2.

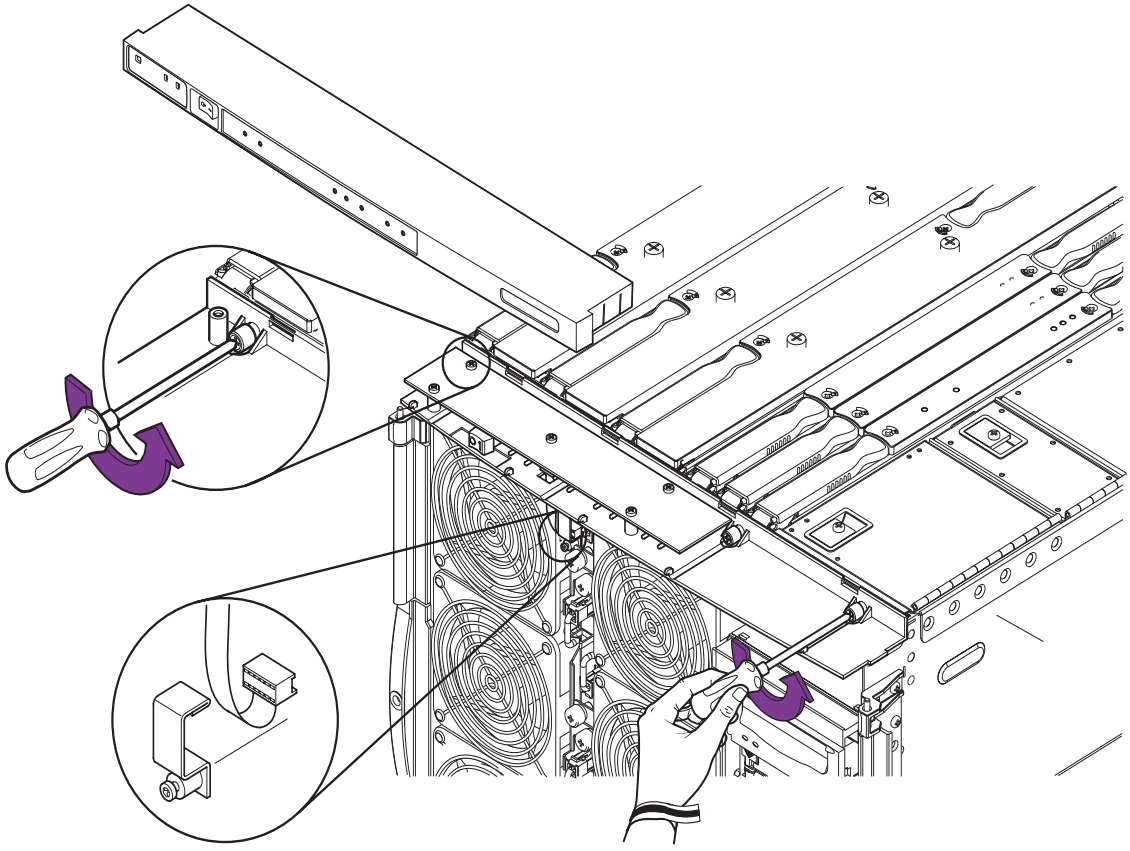


FIGURE 10-2 Removing the System Indicator Board Connector and Securing Screws

6. **Remove the two screws securing the indicator board to the top of the chassis.**

   Refer to FIGURE 10-2.

7. **Remove the module and place it on an ESD mat.**

10.2 Installing the System Indicator Board

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5.

2. **Plug in the indicator board connector to the receptacle at the top of the fan tray and replace the retaining clip.**
3. **Secure the board using the two screws.**
4. **Push the system indicator board housing on to the chassis until the plastic clips engage.**
5. **Close the front doors.**
6. **Remove the wrist strap.**

CHAPTER 11

Baseplane

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

Caution – This procedure requires the system to be extended out of the rack on its slides. Before attempting this procedure you must deploy rack stabilization devices, if fitted.

11.1 To Remove the Baseplane

1. **Power off the system and remove the input power connector(s).**

   Refer to Section 3.3, “Powering Off” on page 3-4.

2. **Deploy the rack stabilization device, if fitted.**

3. **Extend the system from the rack.**

   Loosen the captive screws securing the system to the rack and gently pull it out on its slides.

4. **Attach the wrist strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system. Place a grounded ESD mat close to the system.

5. **Open the front doors.**

6. **Remove the fan tray.**

   Refer to Section 5.2.1, “To Remove the Fan Tray” on page 5-4.

7. **Disengage and raise, but do not completely remove, the following modules:**

   a. **CPU/Memory boards.**

      Refer to Section 7.2.1, “Removing a CPU/Memory Board” on page 7-3.

   b. **Level 2 Repeater boards.**

      Refer to Section 9.1, “Replacing an L2 Repeater Board” on page 9-1.

8. **Remove the following modules completely:**

   a. **IB_SSC board.**

      Refer to Section 8.1.1, “Removing the IB_SSC Assembly” on page 8-1. there is no need to remove the PCI cards.

   b. **Power Distribution Board.**

      Refer to Section 6.3.1, “Removing the Power Distribution Board” on page 6-5.

9. **From beneath the system, loosen completely the 31 screws securing the baseplane to the chassis.**

   You may need to use a stubby screwdriver if the system is mounted low down in the rack. Refer to FIGURE 11-1.

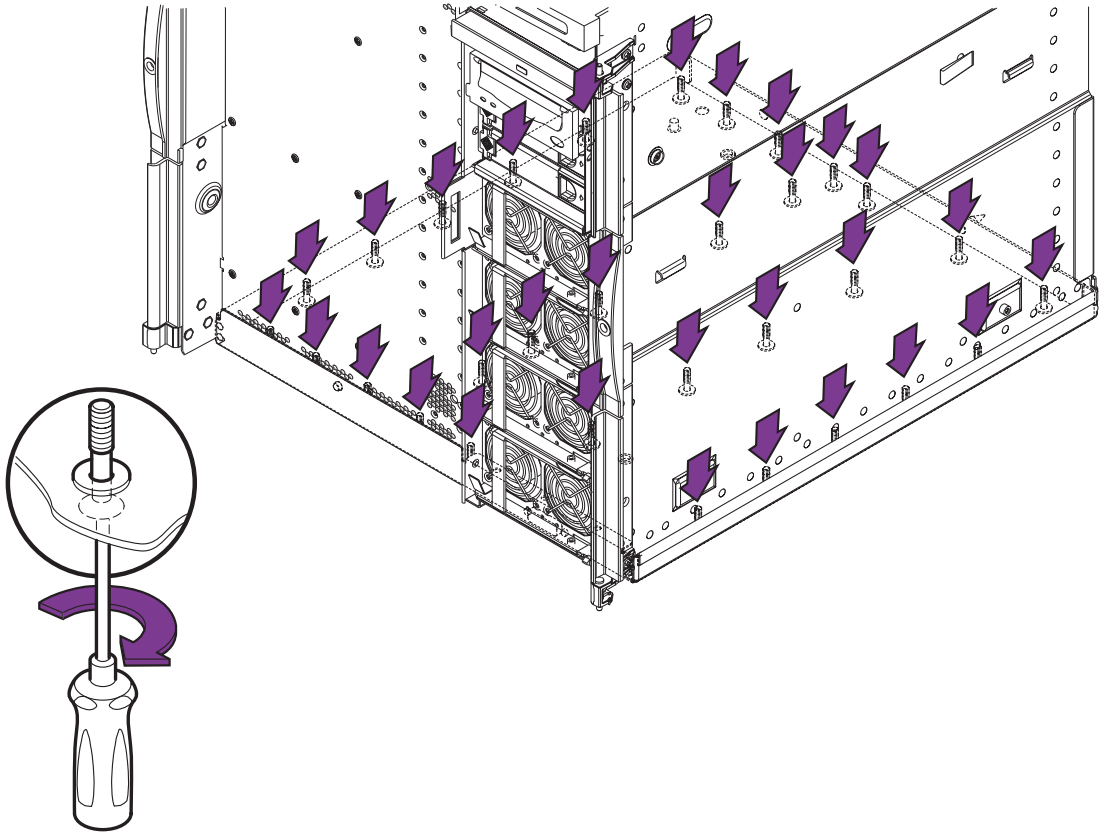


FIGURE 11-1 Removing the 31 Baseplane Securing Screws

10. **With one hand holding the baseplane up, press in the plunger at the front of the chassis.**

Refer to FIGURE 11-2.

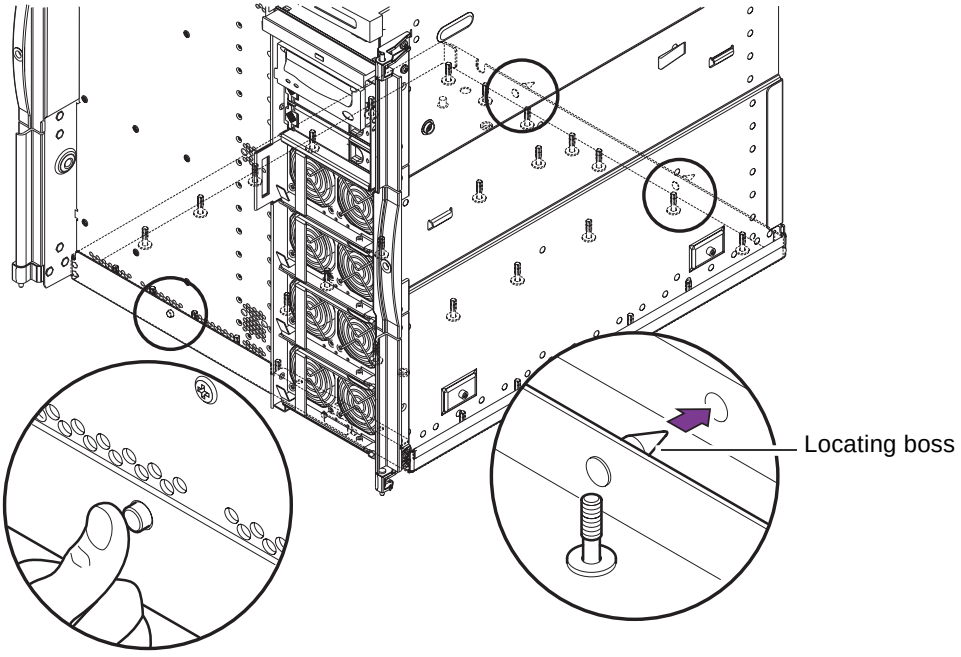


FIGURE 11-2 Releasing the Baseplane Securing Button

11. **Lower the front of the baseplane and pull is forwards to release it from the locating slots at the rear of the chassis.**

Refer to FIGURE 11-2.

12. **Remove the baseplane and place it on an ESD mat.**

    Refer to FIGURE 11-3.

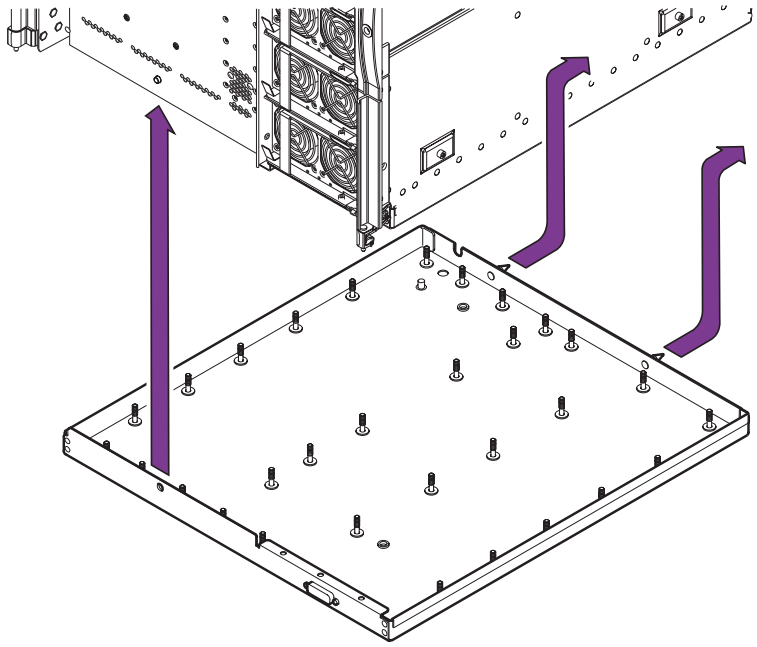


FIGURE 11-3 Removing the Baseplane

11.2 To Install the Baseplane

1. **Attach the wrist strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system. Place a grounded ESD mat close to the system.

2. **Orient the baseplane with the locating bosses to the rear.**

3. **Insert the locating bosses into the slots at the rear of the chassis.**

   Refer to FIGURE 11-2.

4. **Raise the front of the baseplane so that the plunger in the front of the chassis engages in the locating hole in the baseplane.**

5. **Tighten the 31 securing screws beneath the baseplane.**

6. **Carefully re-engage or refit the disengaged and removed modules**:

   a. **Power Distribution Board.**

      Refer to Section 6.3.2, “Installing the Power Distribution Board” on page 6-8.

   b. **IB_SSC board.**

      Refer to Section 8.1.2, “Installing the IB_SSC Assembly” on page 8-4.

   c. **Level 2 Repeater boards.**

      Refer to Section 9.1, “Replacing an L2 Repeater Board” on page 9-1.

   d. **CPU/Memory boards.**

      Refer to Section 7.2.2, “Installing a CPU / Memory Board” on page 7-6.

7. **Reinstall the fan tray.**

   Refer to Section 5.2.2, “To Install the Fan Tray” on page 5-7.

8. **Remove the wrist strap.**

9. **Slide the system into the rack and secure it.**

10. **Retract the the rack stabilization device, if fitted.**

11. **Power on the system.**

    Refer to Section 3.2, “Powering On” on page 3-2.

CHAPTER 12

Antigravity Clutches

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

Caution – This procedure requires the system to be extended out of the rack on its slides. Before attempting this procedure you must deploy rack stabilization devices, if fitted.

The replacement antigravity clutch kit contains three different types of clutch, one for each type of FRU. They can be identified by their part numbers as follows:

- IB_SSC – 370-4858
- CPU / Memory board – 370-4856
- Level 2 Repeater – 370-4857

They are all installed in the same way.

1. **If you are replacing an L2 or CPU/Memory board clutch, power down the system to standby. If you are replacing an IB_SSC clutch you must power down the system completely and remove the input power connectors.**

   Refer to Section 3.3, “Powering Off” on page 3-4.

2. **Extend and lock the rack stabiliser feet (if fitted).**

3. **Slide the system out of the rack.**

   Loosen the captive screws securing the system to the rack and gently pull it out on its slides.

4. **Attach a wrist strap or foot strap.**

   Refer to Section 2.6, “Antistatic Precautions” on page 2-5. Connect the ESD wrist strap or foot strap to the system. Place a grounded ESD mat close to the system.

5. **Remove the module whose clutch is to be replaced.**

   For a CPU/Memory board refer to Section 7.2.1, “Removing a CPU/Memory Board” on page 7-3.

   For the IB_SSC refer to Section 8.1.1, “Removing the IB_SSC Assembly” on page 8-1.

   For an L2 Repeater refer to Section 9.1, “Replacing an L2 Repeater Board” on page 9-1.

6. **Remove the two screws retaining the faulty clutch and remove the clutch.**

7. **Use the screws supplied to secure the new clutch in the same position.**

8. **Replace the module previously removed.**

   For a CPU/Memory board refer to Section 7.2.2, “Installing a CPU/Memory Board” on page 7-6.

   For the IB_SSC refer to Section 8.1.2, “Installing the IB_SSC Assembly” on page 8-4.

   For an L2 Repeater refer to Section 9.1, “Replacing an L2 Repeater Board” on page 9-1.

9. **Remove the antistatic wrist or foot strap.**

10. **Slide the system into the rack and secure it.**

11. **Complete the power-on steps.**

    Refer to Section 3.2, “Powering On” on page 3-2 for complete procedures for powering on the system.

PART IV Appendices

APPENDIX **A**

Parts List

This chapter describes the availability of FRUs and X-options for the Sun Fire V1280 system, and who can perform the upgrade/installation procedures.

Some of the FRUs and X-options can be installed by a competent system administrator, but many *must* be installed by an appropriately qualified service engineer, as shown in TABLE A-1.

TABLE A-1 FRUs and X-Options

				Can be installed by:	
Description	**Configuration**	**X-Option Part Number**	**FRU Part No.**	**System Administrator**	**Qualified Service Engineer**
CPU/Memory module	4 x UltraSPARC III 900 MHz	X7057A	F540-4979		✓
Memory expansion	1 Gbyte (4 x 256 Mbyte)	X7053A	F540-5084		✓
	2 Gbyte (4 x 512 Mbyte)	X7051A	F540-5085		✓
	4 Gbyte (4 x 1 Gbyte)	X7052A	F540-5086		✓
AC Power cord kit	US/Asia (NEMA6-15P)	X321L	N/A	✓	✓
	Europe (CEE 7-VII, DIN VDE 0620)	X322L	N/A	✓	✓
	Denmark (DEMKO 107/10-1973)	X323L	N/A	✓	✓
	Switzerland (SEV 1011-S 24507)	X324L	N/A	✓	✓
	Italy (CEI.23-16-V11)	X325L	N/A	✓	✓
	Australia (AS3112)	X326L	N/A	✓	✓
	UK (BS1363A)	X327L	N/A	✓	✓

TABLE A-1 FRUs and X-Options *(Continued)*

Description	Configuration	X-Option Part Number	FRU Part No.	Can be installed by: System Administrator	Can be installed by: Qualified Service Engineer
	Argentina (IRAM 2073)	X335L	N / A	✓	✓
Cable management arm	CMA-Lite	X1209A	N / A	✓	✓
	CMA-800		F370-5411		
SCSI hard disk drive	36 Gbyte, 10krpm, 1-inch	N / A	F540-4904	✓	✓
DDS-4 tape drive		X6298A	F390-0900		✓
DVD-ROM drive			F370-4412		✓
Environmental filter kit		X6805A		✓	✓
Bezel kit		X7006A		✓	✓
CPU / memory filler board		X1092A			✓
Tape drive blanking panel		X1093A		✓	✓
AC Power supply			F300-1523	✓	✓
Power distribution board			F370-4394		✓
Baseplane			F540-4968		✓
System configuration card reader			F540-4983		✓
Media bay (includes SCSI backplane)			F540-4966		✓
Repeater board			F540-5521		✓
IB_SSC assembly			F540-5290		✓
Main system fans			F540-5193		✓
System fan tray (includes 8 fans)			F540-4972		✓
IB fan			F540-5222		✓
Top bezel and system indicator board			F560-2690		
AC power inlet assembly			F370-4422		

TABLE A-1 FRUs and X-Options *(Continued)*

Description	Configuration	X-Option Part Number	FRU Part No.	Can be installed by: System Administrator	Can be installed by: Qualified Service Engineer
DVD-ROM backplane			F370-4344		
System configuration card			F370-5155		
Cable kit			F560-2686		
Anti-gravity clutch kit			F560-2687		
Rackmount slide kit			F370-5408		
PCI cards					
SCSI	Dual channel differential Ultra / Wide SCSI	X6541A			✓
	SCSI LVD 160 / 320	X6758A			✓
Serial	High speed serial 4-port 2.0	X1155A	F605-1611		✓
	Asynchronous serial 8-port 3.0	X2156A	F605-1644		✓
Ethernet	Quad Fast Ethernet QFE / P	X1034A	F605-1594		✓
	10 / 100 / 1000 Ethernet Category 5 PCI66	X1150A			✓
	Gigabit Ethernet Fibre PCI66	X1151A			✓
ATM	SunATM-155 / MMF 4.0 PCI66	X1157A			✓
	SunATM / P-622MMF 4.0 PCI66	X1159A			✓
	SunATM-155 / MMF 5.0 PCI66	X1201A			✓
	SunATM / P-622MMF 5.0 PCI66	X1210A			✓
Fiber Channel	FC-AL single loop host	X6799A			✓
	FC-AL dual loop host	X6727A			✓
	Redundant DC 8-port switch	X6746A			✓

TABLE A-1 FRUs and X-Options *(Continued)*

Description	Configuration	X-Option Part Number	FRU Part No.	Can be installed by: System Administrator	Can be installed by: Qualified Service Engineer
Combination	Dual Fast Ethernet + Dual SE LVD SCSI	X2222A			✓
Encryption	Encryption	X1133A			✓
	Encryption - Deimos	X1198A			✓
	Encryption - Venus	X1199A			✓
Clustering	Cluster SCSI/PCI	X1074A			✓
Graphics	Graphics	X3668A			✓

APPENDIX **B**

Connector Pinouts

This appendix describes the various cables and connectors which should be made available in order for the installation to be completed.

The Sun Fire V1280 system has the following connectors on the rear:

- Two Gigabit Ethernet RJ45 ports
- Up to six PCI ports (5 x 33 MHz and 1 x 66 MHz)
- Two serial ports (one reserved)
- Alarms port
- 10/100 Ethernet port
- SCSI port

The locations of the ports are shown in FIGURE B-1.

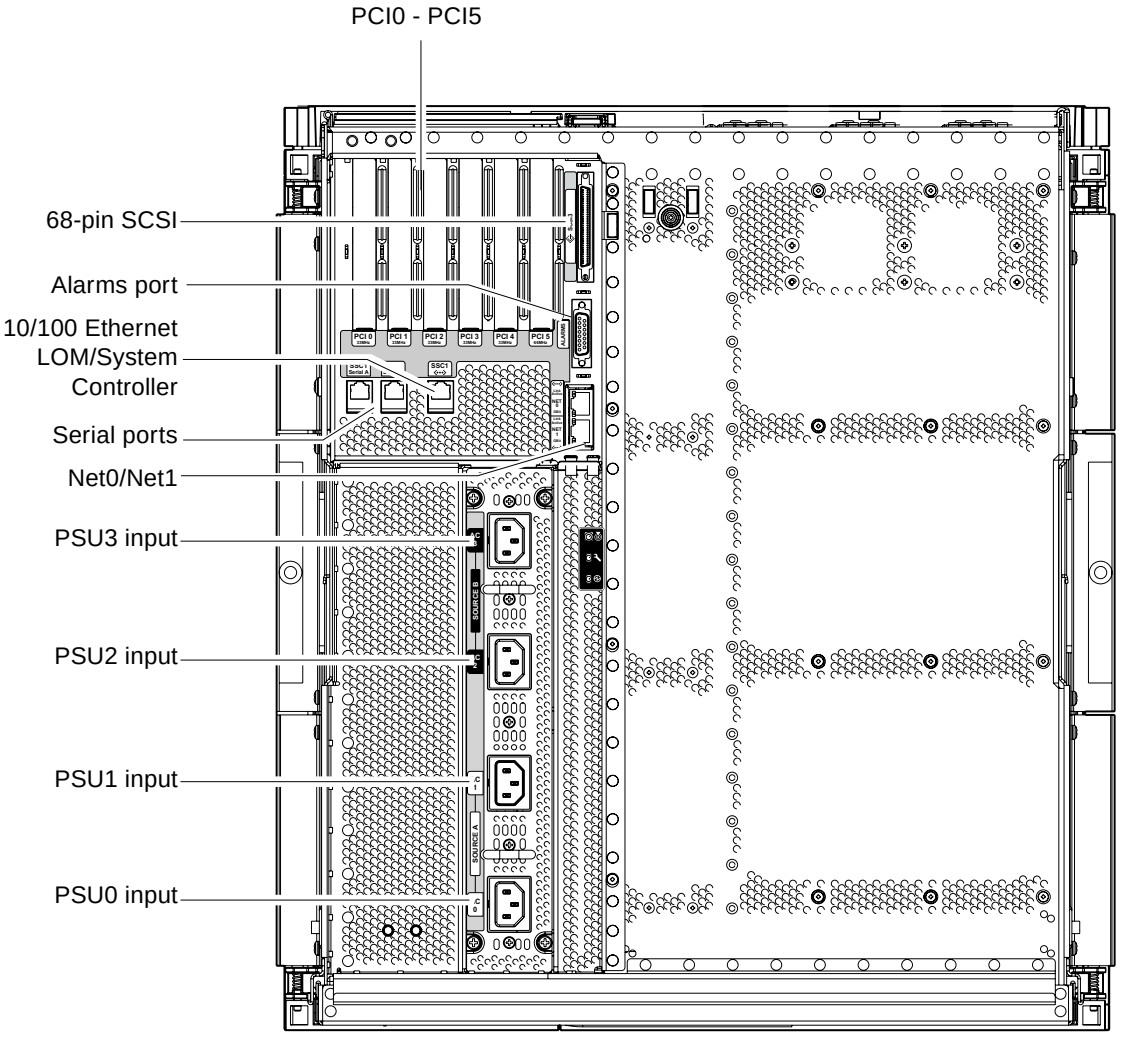


FIGURE B-1 External I/O Connections

B.1 Gigabit Ethernet Connectors

The Gigabit Ethernet connectors are shielded RJ45, and TABLE B-1 lists the connector pinout.

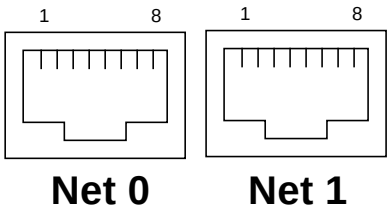


FIGURE B-2 RJ45 Gigabit Ethernet Connectors

TABLE B-1 Gigabit Ethernet Connector Pinout

Pin	Signal Name	Pin	Signal Name
1	TRD0_H	5	TRD2_L
2	TRD0_L	6	TRD1_L
3	TRD1_H	7	TRD3_H
4	TRD2_H	8	TRD3_L

B.2 Serial Connectors

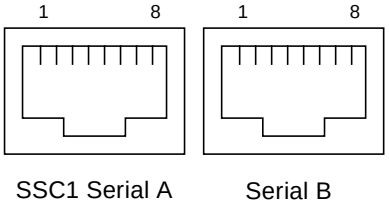


FIGURE B-3 RJ45 Serial Connectors

TABLE B-2 RJ45 Serial Connector Pinout

Pin	Signal
1	RTS
2	DTR
3	TXD
4	Signal Ground
5	Signal Ground
6	RXD
7	DSR
8	CTS

Note – Serial port B is reserved.

B.3 SCSI Connector

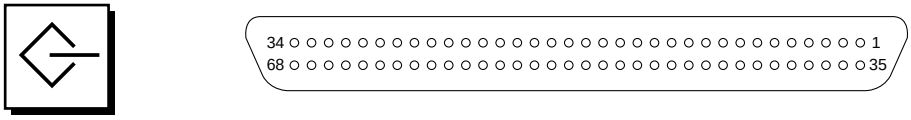


FIGURE B-4 68-Pin SCSI Connector

TABLE B-3 68-pin SCSI Connector Pinout

Pin No.	Signal Name	Type	Pin No.	Signal Name	Type	Pin No.	Signal Name	Type
1	+DB(12)	I/O	24	+ACK	I/O	47	–DB(7)	I/O
2	+DB(13)	I/O	25	+RST	I/O	48	–P_CRCA	I/O
3	+DB(14)	I/O	26	+MSG	I/O	49	Ground	GND
4	+DB(15)	I/O	27	+SEL	I/O	50	Ground	GND
5	+DB(P1)	I/O	28	+C/D	I/O	51	Termpwr	POWER
6	+DB(0)	I/O	29	+REQ	I/O	52	Termpwr	POWER
7	+DB(1)	I/O	30	+I/O	I/O	53	Reserved	NA
8	+DB(2)	I/O	31	+DB(8)	I/O	54	Ground	GND
9	+DB(3)	I/O	32	+DB(9)	I/O	55	–ATN	I/O
10	+DB(4)	I/O	33	+DB(10)	I/O	56	Ground	GND
11	+DB(5)	I/O	34	+DB(11)	I/O	57	–BSY	I/O
12	+DB(6)	I/O	35	–DB(12)	I/O	58	–ACK	I/O
13	+DB(7)	I/O	36	–DB(13)	I/O	59	–RST	I/O
14	+P_CRCA	I/O	37	–DB(14)	I/O	60	–MSG	I/O
15	Ground	GND	38	–DB(15)	I/O	61	–SEL	I/O
16	Diffsens	ANAL	39	–DB(P1)	I/O	62	–C/D	I/O
17	Termpwr	POWER	40	–DB(0)	I/O	63	–REQ	I/O
18	Termpwr	POWER	41	–DB(1)	I/O	64	–I/O	I/O
19	Reserved	NA	42	–DB(2)	I/O	65	–DB(8)	I/O
20	Ground	GND	43	–DB(3)	I/O	66	–DB(9)	I/O
21	+ATN	I/O	44	–DB(4)	I/O	67	–DB(10)	I/O
22	Ground	GND	45	–DB(5)	I/O	68	–DB(11)	I/O
23	+BSY	I/O	46	–DB(6)	I/O			

Note – All signals shown in TABLE B-3 are active low.

B.3.1 SCSI Implementation

- SCSI Fast-160 (UltraSCSI) low-voltage differential parallel interface
  - 16-bit SCSI bus
  - 160Mbps data transfer rate
- Support for 16 SCSI addresses:
  - Target 0 to 6 and 8 to F for devices
  - Target 7 reserved for SCSI host adapter on main logic board
- Support for up to three internal SCSI devices (plus the host adapter) (on a second SCSI bus):
  - Disk 0[0]
  - Disk 1[1]
  - Tape [5]
- Maximum cable length 25 meters (terminator to terminator) for low-voltage differential, point-to-point interconnect.

B.4 10 / 100 LOM / System Controller Ethernet Connector

FIGURE B-5 RJ45 TPE Socket

TABLE B-4 TPE Connector Pinout

Pin	Description	Pin	Description
1	TXD+	5	Common mode termination
2	TXD–	6	RXD–
3	RXD+	7	Common mode termination
4	Common mode termination	8	Common mode termination

B.4.1 TPE Cable-Type Connectivity

The following types of twisted-pair Ethernet cable can be connected to the 8-pin TPE connector:

- For 10BASE-T applications, shielded twisted-pair (STP) cable:
  - Category 3 (STP-3, *voice* grade)
  - Category 4 (STP-4)
  - Category 5 (STP-5, *data* grade)
- For 100BASE-T applications, shielded twisted-pair category 5 (STP-5, *data* grade) cable.

TABLE B-5 TPE STP-5 Cable Lengths

Cable Type	Application(s)	Max Length (Metric)	Max Length (Imperial)
Shielded twisted pair category 5 (STP-5, *data* grade)	10BASE-T	1000m	3282ft
Shielded twisted pair category 5 (STP-5, *data* grade)	100BASE-T	100m	327ft

B.5 Alarms Port

The alarms service port connector is a male DB-15. TABLE B-6 lists the pinout.

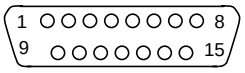


FIGURE B-6 DB-15 (Male) Alarms Service Port Connector

TABLE B-6 Alarms Service Port Connector Pinout

Pin	Signal Name	Description	State
1	Not connected		
2	Not connected		
3	Not connected		
4	Not connected		
5	SYSTEM_NO	UNIX Running	Normally open
6	SYSTEM_NC	UNIX Running	Normally closed
7	SYSTEM_COM	UNIX Running	Common
8	ALARM1_NO	Alarm1	Normally open
9	ALARM1_NC	Alarm1	Normally closed
10	ALARM1_COM	Alarm1	Common
11	ALARM2_NO	Alarm2	Normally open
12	ALARM2_NC	Alarm2	Normally closed
13	ALARM2_COM	Alarm2	Common
14	Not connected		
15	Not connected		

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