Features

- **Compatible with MCS-51™ Products**
- **128K Bytes of In-System Reprogrammable Flash data memory and 4K Bytes of Downloadable Flash Program Memory**
  - **Endurance: 1,000 Write/Erase Cycles per Sector**
  - **Data Retention: 10 Years**
- **Sector Programming: 128 Bytes/Sector**
- **Single 3.3V ± 10% Supply**
- **On-Chip 12 MHz oscillator**
- **Two-Level Program Memory Lock**
- **256-Bytes Internal RAM**
- **5 Programmable I/O Lines**
- **Serial Peripheral Interface (SPI) Channel**
- **Serial Program Downloading**
- **Dual Data Pointer Registers**

Description

The AT89S4D12 is a low-voltage, highly integrated CMOS 8-bit microcomputer with 4K bytes of downloadable Flash program memory and 128K bytes of in-system reprogrammable Flash data memory. The device is manufactured using Atmel's high density Flash memory technology and is compatible with the industry-standard MCS-51™ instruction set.

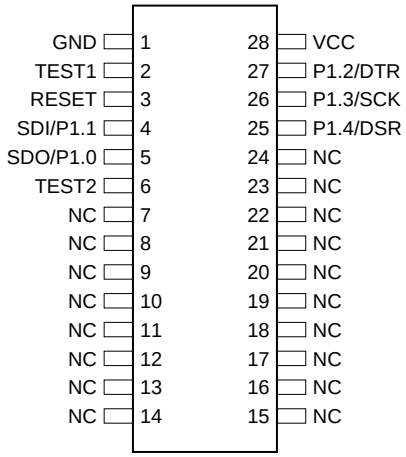
The 128K bytes of on-chip Flash data memory are accessed as two 64K byte blocks. Bit 0 at SFR location 96H is used to select the active block. The MOVX instruction is used to read and write the data memory. Both the program and data memory arrays can be programmed by an external programmer.

The downloadable Flash can be changed one page (128 bytes) at a time and is accessible through the SPI serial peripheral interface port. Holding RESET active forces the SPI bus into a slave input mode and allows the program memory to be written-from or read-to unless Lock Bit 2 has been activated.

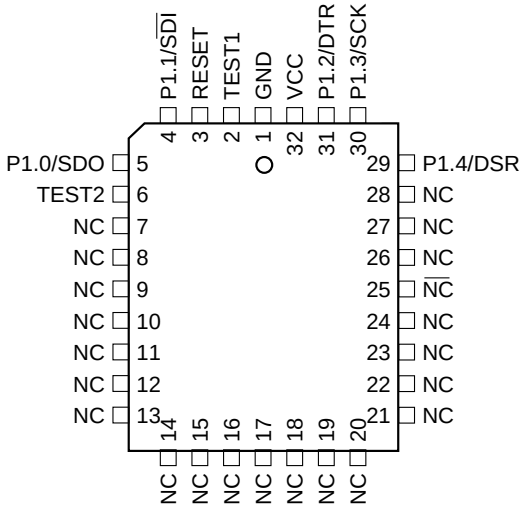
The functional operations of the 128K bytes Flash data memory are equivalent to those on the AT29LV010A 1M Bit Flash memory device.

Pin Configurations

SOIC Top View



PLCC Top View

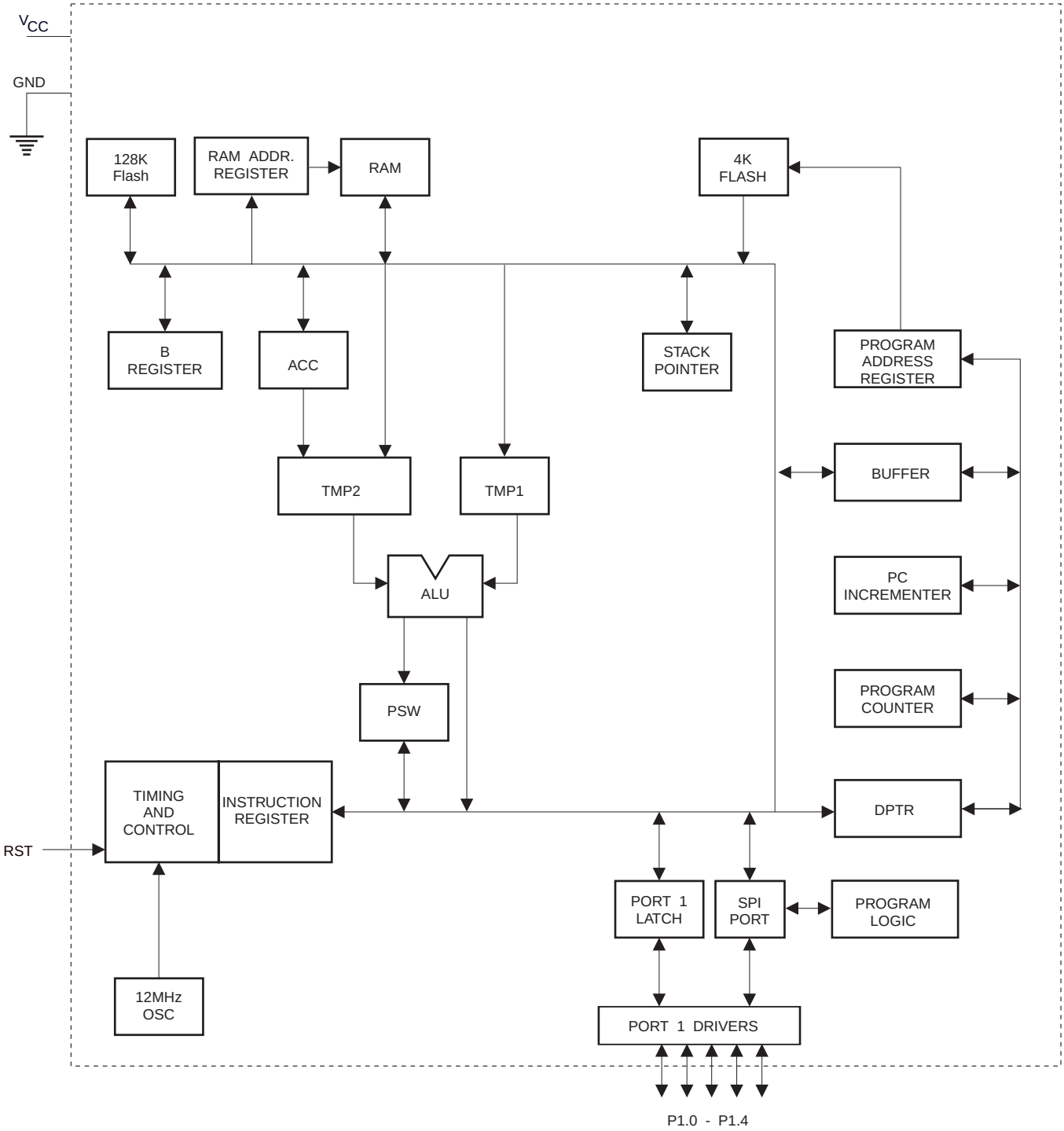


8-Bit Microcontroller with 132K Bytes Flash Data Memory

AT89S4D12

0921A-A–12/97

Block Diagram



Pin Description

V_{CC}
Supply voltage.

GND
Ground.

Port 1
Port 1 is a 5-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

In addition, P1.0, P1.1, and P1.3 can be configured as the SPI data output, data input and shift clock input pins, as shown in the following table.

Port Pin	Alternate Functions
P1.0	SDO (data output pin for SPI channel)
P1.1	SDI (data input pin for SPI channel)
P1.3	SCK (clock input pin for SPI channel)

RST
Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

TEST1
TEST1 is set to V_{CC} during downloading of the Flash program or data memory. This pin can be left unconnected or tied to ground during normal operation.

TEST2
Test input. This pin has no user available function and can be left unconnected or tied to ground.

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Memory Control Register The MCON register contains the RDY/$\overline{\text{BSY}}$ flag and the most significant Flash address bit A16, for the 128K bytes of on-chip Flash data memory.

SPI Registers Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (shown in Table 3) and SPSR (shown in Table 4). The SPI data bits are contained in the SPDR register. Writing the SPI data register during serial data transfer sets the Write Collision bit, WCOL, in the SPSR register. The SPDR is double buffered for writing and the values in SPDR are not changed by Reset.

Dual Data Pointer Registers To facilitate data transfer, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H - 83H and DP1 at 84H - 85H. Bit DPS = 0 in SFR MCON selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer register.

Table 1. AT89S4D12 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000					SPCR 000X01XX			0D7H
0C8H									0CFH
0C0H									0C7H
0B8H									0BFH
0B0H									0B7H
0A8H			SPSR 00000000						0AFH
0A0H									0A7H
98H									9FH
90H	P1 XXX11111						MCON XXXXX010		97H
88H									8FH
80H			DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 0000000	SPDR XXXXXXXX	PCON 0XXX0000	87H

Table 2. MCON—Memory Control Register

MCON Address = 96H — Reset Value = XXXX X010B

	-	-	-	-	-	DPS	RDY/$\overline{BSY}$	A16
Bit	7	6	5	4	3	2	1	0

Symbol	Function
DPS	Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the second bank, DP1.
RDY/$\overline{BSY}$	DataFlash Ready/$\overline{Busy}$ Flag. This bit serves as the RDY/$\overline{BSY}$ flag in a Read-Only mode during DataFlash write. RDY/$\overline{BSY}$ = 1 means that the DataFlash is ready to be programmed. While programming operations are being executed, the RDY/$\overline{BSY}$ bit equals `0' and is automatically reset to `1' when programming is completed.
A16	Memory Block Select. A16 = 0 selects the lower 64K bytes DataFlash memory block. A16 = 1 selects the upper 64K bytes DataFlash block.

Table 3. SPCR—SPI Control Register

SPCR Address = D5H — Reset Value = 000X 01XXB

	SPIE	SPE	DORD	-	CPOL	CPHA	SPR1	SPR0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SPIE	SPI Interrupt Enable. This bit, enables SPI interrupts: SPIE = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
SPE	SPI Enable. SPI = 1 enables the SPI channel and connects SDO, SDI and SCK to pins P1.0, P1.1, and P1.3. SPI = 0 disables the SPI channel.
DORD	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
CPOL	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.
CPHA	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.
SPR0 SPR1	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, F_{OSC}., is as follows: SPR1 — SPR0 — SCK = F_{OSC}. divided by 0 — 0 — 4 0 — 1 — 16 1 — 0 — 64 1 — 1 — 128

Table 4. SPSR—SPI Status Register

SPCR Address = AAH — Reset Value = 000X 0000B

	SPIF	WCOL	—	—	—	—	—	—
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SPIF	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then accessing the SPI data register.
WCOL	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

Table 5. SPDR—SPI Data Register

SPDR Address = 86H — Reset Value = unchanged

	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
Bit	7	6	5	4	3	2	1	0

Data Memory—Flash and RAM

The AT89S4D12 implements 128K bytes of on-chip Flash for data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128-bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 086H (which is SPDR).

MOV 086H, #data

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 086H, accesses the data byte at address 086H, rather than SPDR (whose address is 086H).

MOV @R0, #data

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

The MOVX instructions are used to access the Flash data memory.

Flash write cycles are self-timed and typically take 5 ms per 128-byte page. The progress of Flash write can be monitored by reading the RDY/$\overline{BSY}$ bit (read-only) in SFR MCON. RDY/$\overline{BSY}$ = 0 means programming is still in progress and RDY/$\overline{BSY}$ = 1 means Flash write cycle is completed and another write cycle can be initiated.

Serial Peripheral Interface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S4D12 and an SPI master. The AT89S4D12 SPI features include the following:

- Full-Duplex, 3-Wire Synchronous Data Transfer
- 2 MHz Bit Frequency (max.)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates
- End of Transmission Interrupt Flag
- Write Collision Flag Protection

The interconnection between master and slave CPU with SPI is shown in the following figure. The SCK pin is the clock input. Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the SDI pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If the SPI interrupt enable bit (SPIE) is set, an interrupt is requested.

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figure 3 and Figure 4.

Figure 1. SPI Block Diagram

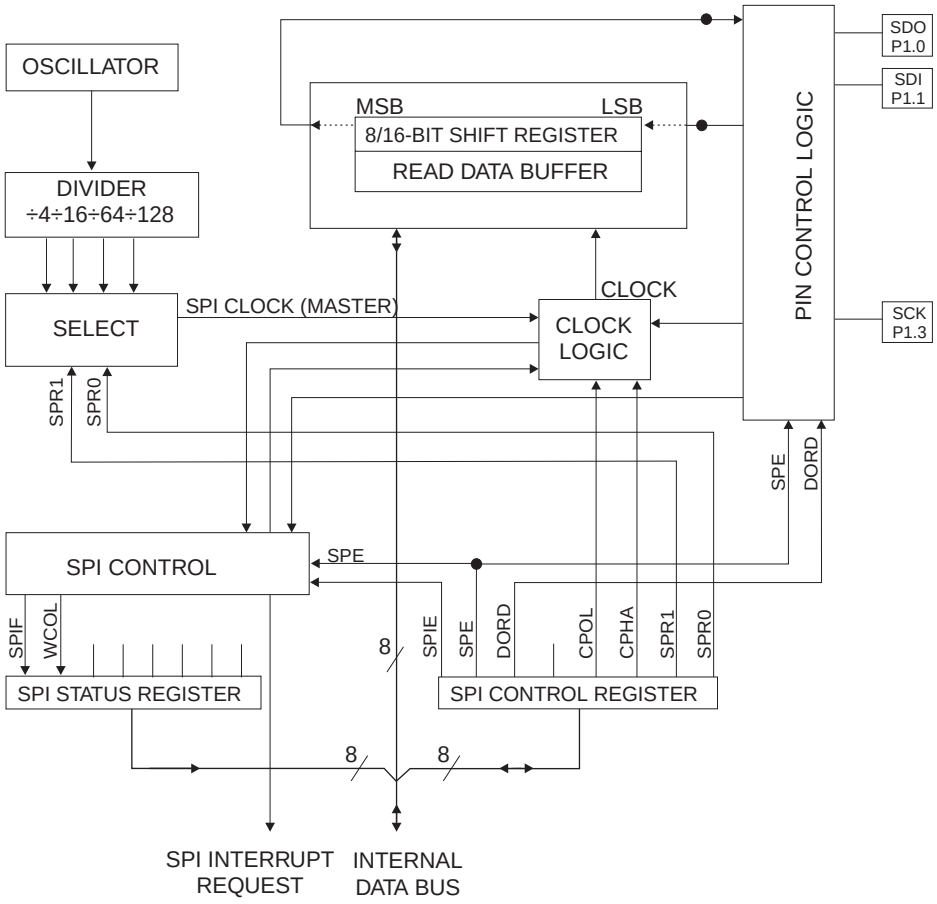


Figure 2. SPI Master - Slave Interconnection

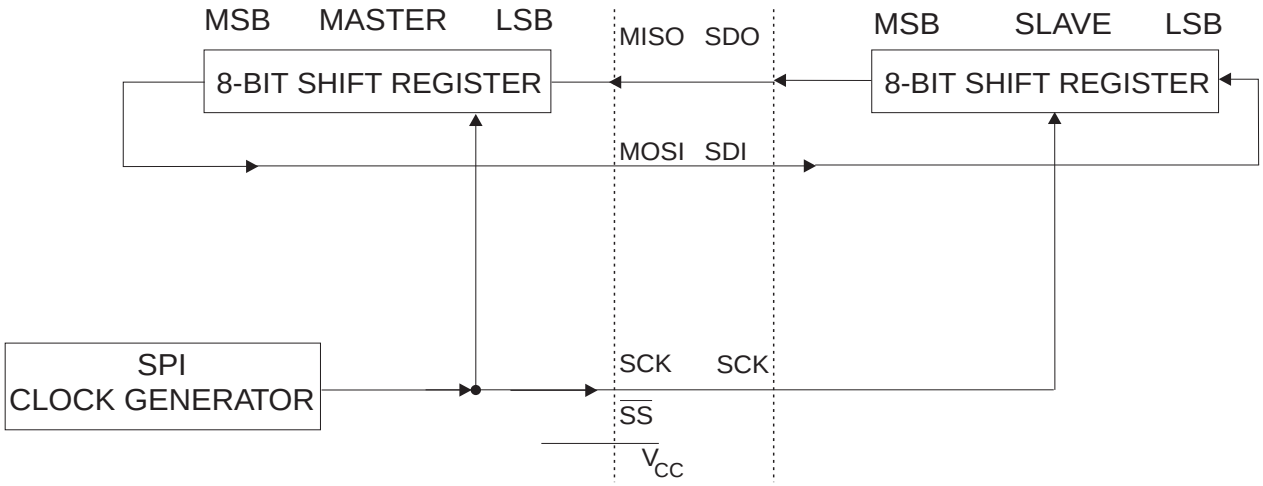
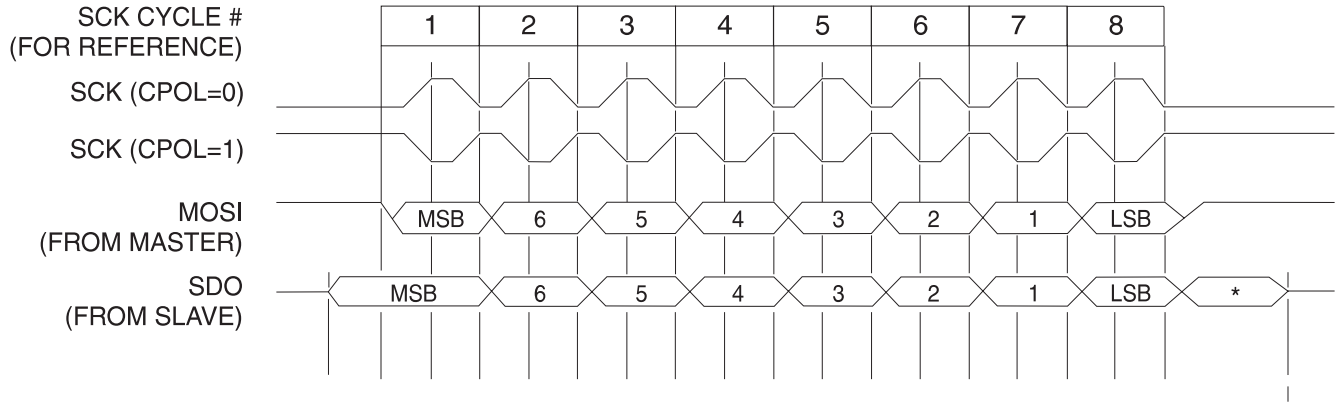
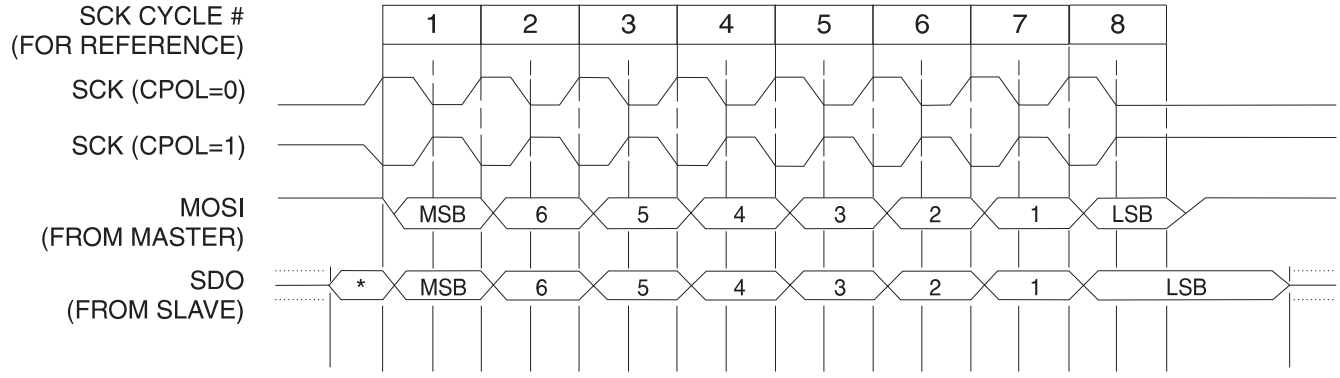


Figure 3. SPI Transfer Format with CPHA = 0



* Not defined but normally MSB of character just received.

Figure 4. SPI Transfer Format with CPHA = 1



* Not defined but normally LSB of previously transmitted character.

Oscillator Characteristics

An on-chip oscillator is provided with a minimum frequency of 12 MHz and maximum frequency of 15 MHz over the recommended operating conditions.

Each CPU instruction cycle takes 12 oscillator cycles.

Program Memory Lock Bits

The AT89S4D12 has two lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table. The self-timed lock bit programming operation typically takes 40 ms.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operation.

Lock Bit Protection Modes(1)(2)

Program Lock Bits			
	LB1	LB2	Protection Type
1	U	U	No internal memory lock feature.
2	P	U	Programming of the Flash memory is disabled.
3	P	P	Same as mode 2, but verify is also disabled.

Notes: 1. U = Unprogrammed
2. P = Programmed

Flash Programming Specification

Both the 128K bytes Data and 4K bytes Code flash memory arrays can be programmed using the serial SPI bus while the RESET and TEST1 pins are pulled to V_{CC} = 3.3V (±10%). Both memory arrays are organized in 128-byte sectors for programming and are written sector-by-sector, similar to the Atmel AT29LV010A.

The serial interface consists of pins SCK (serial shift clock), SDI (serial input) and SDO (serial output). After RESET and TEST1 are set high, the Programming Enable instruction needs to be executed once before programming operations can occur. During device programming, pin TEST2 should be connected to Ground.

An auto-erase cycle is built into the self-timed Page Write operation and there is no need to first execute the Chip Erase instruction. The Chip Erase operation is self-timed and typically takes 5 ms. Chip Erase turns the content of every flash memory location in both the Code and Data arrays into FFH.

The Code and Data memory arrays have separate address spaces: 0000H to 0FFFH for Code memory and 00000H to 2FFFFH for Data memory.

The maximum serial clock (SCK) frequency used during flash programming should be less than 500 KHz. The High time of SCK should be 1.5 µs minimum and Low time should be 0.5 µs minimum.

$\overline{\text{DATA}}$ Polling

The AT89S4D12 features $\overline{\text{DATA}}$ Polling to indicate the end of a page write cycle. During a write cycle, an attempted serial read of the last byte written will result in the complement of the written datum at bit D7. Once the write cycle has been completed, true data are valid on all output data bits, and the next write cycle may begin. $\overline{\text{DATA}}$ Polling may begin any time after a write instruction has been executed.

Toggle Bit

The Toggle Bit provides another method to detect completion of a programming cycle. During a page write or chip erase operation, successive attempts to read data from the memory will result in output bit D6 toggling between '1' and '0'. Once the program cycle has completed, output data bit D6 will stop toggling and valid data will be presented. Examining the toggle bit may begin any time during a program cycle.

Ready/$\overline{\text{Busy}}$

A third method to monitor the progress of programming is provided by the RDY/$\overline{\text{BSY}}$ output signal. Pin P1.4/DSR is pulled Low during programming to indicate $\overline{\text{BUSY}}$ and is pulled High again when programming is done to indicate READY.

Page Write

The Code and Data memory arrays are programmed on a sector basis. If a byte of data is to be changed, data for the entire 128-byte sector must be serially loaded into the device using the appropriate serial interface instruction. The data in any byte that is not loaded during the programming of its sector will be indeterminate. The AT89S4D12 automatically does a sector erase to turn the whole sector into FFH prior to loading the data into the sector. An erase command is not required. The self-timed Page Write cycle typically takes 5 ms (t_{WC}).

(continued)

Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the self-timed programming cycle (t_{WC}). After the first data byte has been loaded into the device, successive bytes need to be entered within 300-µs time intervals. If a Page Write instruction is not detected in 300-µs after the last write instruction, the load period will end and the internal programming cycle will start.

Address bits A7 - A11 and A7 - A16 specify the sector address of the Code and Data memory arrays, respectively. The valid sector address must be entered during each write instruction. Address bits A0 - A6 specify the byte address within the sector. The bytes may be loaded in any order, sequential loading is not required. Once a programming operation has been initiated, and for a duration of typically 5 ms, a read operation will effectively be a polling operation.

Program Verify

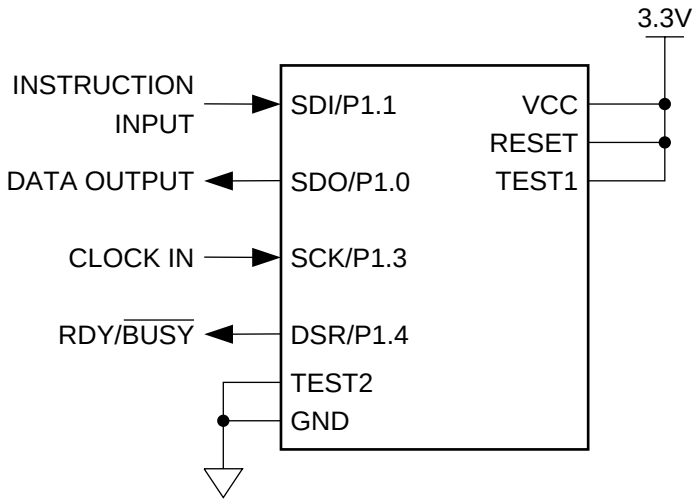
If lock bits LB1 and LB2 have not been programmed, the programmed Code and Data byte can be read back via serial output pin SDO. The state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

Serial Programming Instruction Set

Instruction	Format				Operation
	Byte 1	Byte 2	Byte 3	Byte 4	
Programming Enable	10101100	01010011	11111111	11111111	Enable Serial Programming after RST goes high.
Chip Erase	10101100	10000000	xxxxxxxx	xxxxxxxx	Chip erase both 128K & 4K memory arrays.
Read Code Memory	0010000x	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	DDDDDDDD	Read data at pin SDO for Code memory at address A11:A0.
Page Write Code Memory	0100000x	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	DDDDDDDD	Write data at pin SDI for Code memory at address A11:A0.
Read Data Memory	1010000 A16	A15 A14 A13 A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	DDDDDDDD	Read data at pin SDO for Data memory at address A16:A0.
Page Write Data Memory	1100000 A16	A15 A14 A13 A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	DDDDDDDD	Write data at pin SDI for Data memory at address A16:A0.
Program Lock Bits	10101100	111000 LB2 LB1	xxxxxxxx	xxxxxxxx	Set LB1, LB2 = '0' to program lock bits.
Read Signature	0011000x	xxxxxxxx	x A6 A5 A4 A3 A2 A1 A0	DDDDDDDD	Read device I.D. at address A6:A0.

Notes:
1. A16:A0 = Memory byte address
2. 'DDDDDDDD' = Data input at pin SDI or data output at pin SDO.
3. 'x' = Don't care.

Flash Memory Serial Programming Circuit



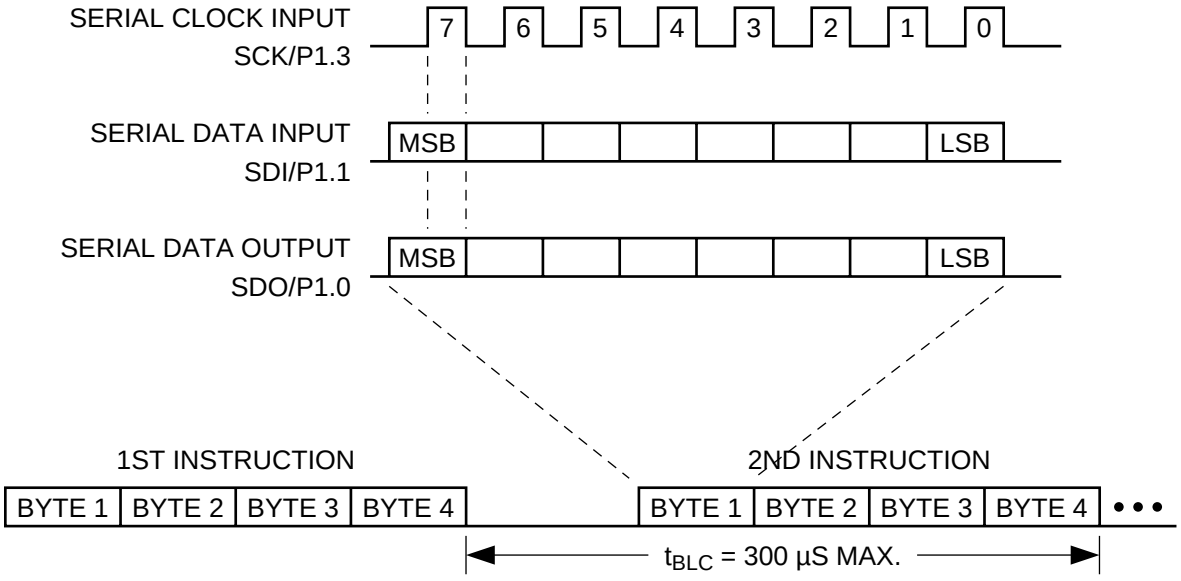
Reading the Signature Bytes

The signature bytes are read by executing the Read Signature command at locations 30H and 31H. The values returned are as follows:

(30H) = 1EH indicates manufactured by Atmel

(31H) = 84H indicates AT89S4D12

Serial Downloading Waveforms



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.0V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 3.0V to 3.6V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage		-0.5	0.2 V_{CC} - 0.1	V
V_{IH}	Input High Voltage	(Except RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High Voltage	(RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage(1)	I_{OL} = 1.6 mA		0.5	V
V_{OH}	Output High Voltage	I_{OH} = -60 µA	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current	V_{IN} = 2V		-650	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode		20	mA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 5 bit port: 15 mA
If I_{OL} exceeds the test condition, V_{OL} may exceeed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power Down is 2V.

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	3.3V ± 10%	AT89S4D12-12JC AT89S4D12-12RC	32J 28R	Commercial (0°C to 70°C)
		AT89S4D12-12JI AT89S4D12-12RI	32J 28R	Industrial (-40°C to 85°C)

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
28R	28-Lead, Plastic Gull Wing Small Outline (SOIC)