

CMOS, the Ideal Logic Family

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Stephen Calebotta
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CMOS, the Ideal Logic Family

INTRODUCTION

Let's talk about the characteristics of an ideal logic family. It should dissipate no power, have zero propagation delay, controlled rise and fall times, and have noise immunity equal to 50% of the logic swing.

The properties of CMOS (complementary MOS) begin to approach these ideal characteristics.

First, CMOS dissipates low power. Typically, the static power dissipation is 10 nW per gate which is due to the flow of leakage currents. The active power depends on power supply voltage, frequency, output load and input rise time, but typically, gate dissipation at 1 MHz with a 50 pF load is less than 10 mW.

Second, the propagation delays through CMOS are short, though not quite zero. Depending on power supply voltage, the delay through a typical gate is on the order of 25 ns to 50 ns.

Third, rise and fall times are controlled, tending to be ramps rather than step functions. Typically, rise and fall times tend to be 20 to 40% longer than the propagation delays.

Last, but not least, the noise immunity approaches 50%, being typically 45% of the full logic swing.

Besides the fact that it approaches the characteristics of an ideal logic family and besides the obvious low power battery applications, why should designers choose CMOS for new systems? The answer is cost.

On a component basis, CMOS is still more expensive than TTL. However, system level cost may be lower. The power supplies in a CMOS system will be cheaper since they can be made smaller and with less regulation. Because of lower currents, the power supply distribution system can be simpler and therefore, cheaper. Fans and other cooling equipment are not needed due to the lower dissipation. Because of longer rise and fall times, the transmission of digital signals becomes simpler making transmission techniques less expensive. Finally, there is no technical reason why CMOS prices cannot approach present day TTL prices as sales volume and manufacturing experience increase. So, an engineer about to start a new design should compare the system level cost of using CMOS or some other logic family. He may find that, even at today's prices, CMOS is the most economical choice.

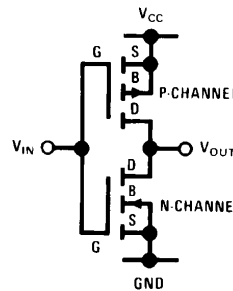
National is building two lines of CMOS. The first is a number of parts of the CD4000A series. The second is the 54C/74C series which National introduced and which will become the industry standard in the near future.

The 54C/74C line consists of CMOS parts which are pin and functional equivalents of many of the most popular parts in the 7400 TTL series. This line is typically 50% faster than the 4000A series and sinks 50% more current. For ease of design, it is spec'd at TTL levels as well as CMOS levels, and there are two temperature ranges available: 54C, -55°C to +125°C or 74C, -40°C to +85°C. Table I compares the port parameters of the 54C/74C CMOS line to those of the 54L/74L low power TTL line.

CHARACTERISTICS OF CMOS

The aim of this section is to give the system designer not familiar with CMOS, a good feel for how it works and how it behaves in a system. Much has been written about MOS devices in general. Therefore, we will not discuss the design and fabrication of CMOS transistors and circuits.

The basic CMOS circuit is the inverter shown in *Figure 2-1*. It consists of two MOS enhancement mode transistors, the upper a P-channel type, the lower an N-channel type.



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FIGURE 2-1. Basic CMOS Inverter

The power supplies for CMOS are called V_{DD} and V_{SS} , or V_{CC} and Ground depending on the manufacturer. V_{DD} and V_{SS} are carryovers from conventional MOS circuits and stand for the drain and source supplies. These do not apply directly to CMOS since both supplies are really source supplies. V_{CC} and Ground are carryovers from TTL logic and that nomenclature has been retained with the introduction of the 54C/74C line of CMOS. V_{CC} and Ground is the nomenclature we shall use throughout this paper.

The logic levels in a CMOS system are V_{CC} (logic "1") and Ground (logic "0"). Since "on" MOS transistor has virtually no voltage drop across it if there is no current flowing through it, and since the input impedance to CMOS device

TABLE I. Comparison of 54L/74L Low Power TTL and 54C/74C CMOS Port Parameters

Family	V _{CC}	V _{IL} Max	I _{IL} Max	V _{IH} Min	I _{IH} 2.4V	V _{OL} Max	I _{OL}	V _{OH} Min	I _{OH}	t _{pd0} Typ	t _{pd1} Typ	P _{DISS/Gate} Static	P _{DISS/Gate} 1 MHz, 50 pF Load
54L/74L	5	0.7	0.18 mA	2.0	10 μA	0.3	2.0 mA	2.4	100 μA	31	35	1 mW	2.25 mW
54C/74C	5	0.8	—	3.5	—	0.4	*360 μA	2.4	*100 μA	60	45	0.00001 mW	1.25 mW
54C/74C	10	2.0	—	8.0	—	1.0	**10 μA	9.0	**10 μA	25	30	0.00003 mW	5 mW

*Assumes interfacing to low power TTL.

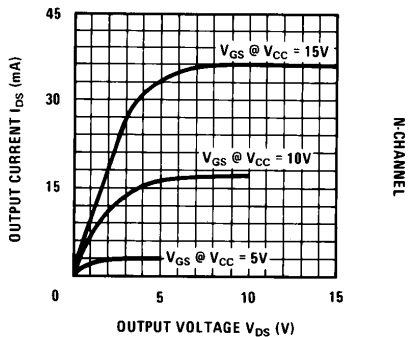
**Assumes interfacing to CMOS.

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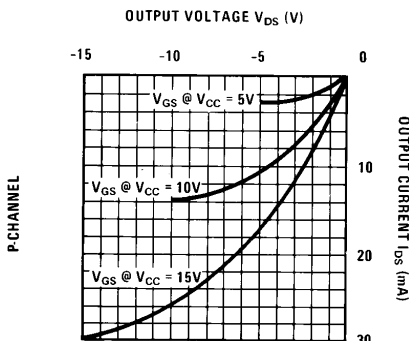
is so high (the input characteristic of an MOS transistor is essentially capacitive, looking like a $10^{12}\Omega$ resistor shunted by a 5 pF capacitor), the logic levels seen in a CMOS system will be essentially equal to the power supplies.

Now let's look at the characteristic curves of MOS transistors to get an idea of how rise and fall times, propagation delays and power dissipation will vary with power supply voltage and capacitive loading. Figure 2-2 shows the characteristic curves of N-channel and P-channel enhancement mode transistors.

There are a number of important observations to be made from these curves. Refer to the curve of $V_{GS} = 15V$ (Gate to Source Voltage) for the N-channel transistor. Note that for a constant drive voltage V_{GS} , the transistor behaves like a current source for V_{DS} 's (Drain to Source Voltage) greater than $V_{GS} - V_T$ (V_T is the threshold voltage of an MOS transistor). For V_{DS} 's below $V_{GS} - V_T$, the transistor behaves essentially like a resistor. Note also that for lower V_{GS} 's, there are similar curves except that the magnitude of the I_{DS} 's are significantly smaller and that in fact, I_{DS} increases approximately as the square of increasing V_{GS} . The P-channel transistor exhibits essentially identical, but complemented, characteristics.



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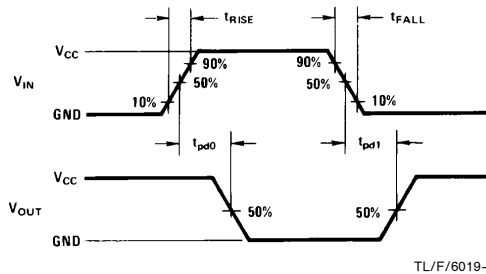
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FIGURE 2-2. Logical "1" Output Voltage vs Source Current

If we try to drive a capacitive load with these devices, we can see that the initial voltage change across the load will be ramp-like due to the current source characteristic followed by a rounding off due to the resistive characteristic dominating as V_{DS} approaches zero. Referring this to our basic CMOS inverter in Figure 2-1, as V_{DS} approaches zero, V_{OUT} will approach V_{CC} or Ground depending on whether the P-channel or N-channel transistor is conducting.

Now if we increase V_{CC} and, therefore, V_{GS} the inverter must drive the capacitor through a larger voltage swing. However, for this same voltage increase, the drive capability (I_{DS}) has increased roughly as the square of V_{GS} and, therefore, the rise times and the propagation delays through the inverter as measured in Figure 2-3 have decreased.

So, we can see that for a given design, and therefore fixed capacitive load, increasing the power supply voltage will increase the speed of the system. Increasing V_{CC} increases speed but it also increases power dissipation. This is true for two reasons. First, CV^2f power increases. This is the power dissipated in a CMOS circuit, or any other circuit for that matter, when driving a capacitive load.



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FIGURE 2-3. Rise and Fall Times and Propagation Delays as Measured in a CMOS System

For a given capacitive load and switching frequency, power dissipation increases as the square of the voltage change across the load.

The second reason is that the VI power dissipated in the CMOS circuit increases with V_{CC} (for V_{CC} 's $> 2V_T$). Each time the circuit switches, a current momentarily flows from V_{CC} to Ground through both output transistors. Since the threshold voltages of the transistors do not change with increasing V_{CC} , the input voltage range through which the upper and lower transistors are conducting simultaneously increases as V_{CC} increases. At the same time, the higher V_{CC} provides higher V_{GS} voltages which also increase the magnitude of the I_{DS} currents. Incidentally, if the rise time of the input signal was zero, there would be no current flow from V_{CC} to Ground through the circuit. This current flows because the input signal has a finite rise time and, therefore, the input voltage spends a finite amount of time passing through the region where both transistors conduct simultaneously. Obviously, input rise and fall times should be kept to a minimum to minimize VI power dissipation.

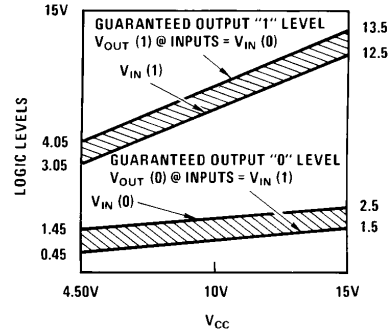
Let's look at the transfer characteristics, Figure 2-4, as they vary with V_{CC} . For the purposes of this discussion we will assume that both transistors in our basic inverter have identical but complementary characteristics and threshold voltages. Assume the threshold voltages, V_T , to be 2V. If V_{CC} is

less than the threshold voltage of 2V, neither transistor can ever be turned on and the circuit cannot operate. If V_{CC} is equal to the threshold voltage exactly then we are on the curve shown in Figure 2-4a. We appear to have 100% hysteresis. However, it is not truly hysteresis since both output transistors are off and the output voltage is being held on the gate capacitances of succeeding circuits. If V_{CC} is somewhere between one and two threshold voltages (Figure 2-4b), then we have diminishing amounts of "hysteresis" as we approach V_{CC} equal to $2V_T$ (Figure 2-4c). At V_{CC} equal to two thresholds we have no "hysteresis" and no current flow through both the upper and lower transistors during switching. As V_{CC} exceeds two thresholds the transfer curves begin to round off (Figure 2-4d). As V_{IN} passes through the region where both transistors are conducting, the currents flowing through the transistors cause voltage drops across them, giving the rounded characteristic.

Considering the subject of noise in a CMOS system, we must discuss at least two specs: noise immunity and noise margin.

National's CMOS circuits have a typical noise immunity of $0.45 V_{CC}$. This means that a spurious input which is $0.45 V_{CC}$ or less away from V_{CC} or Ground typically will not propagate through the system as an erroneous logic level. This does not mean that no signal at all will appear at the output of the first circuit. In fact, there will be an output signal as a result of the spurious input, but it will be reduced in amplitude. As this signal propagates through the system, it will be attenuated even more by each circuit it passes through until it finally disappears. Typically, it will not change any signal to the opposite logic level. In a typical flip flop, a $0.45 V_{CC}$ spurious pulse on the clock line would not cause the flop to change state.

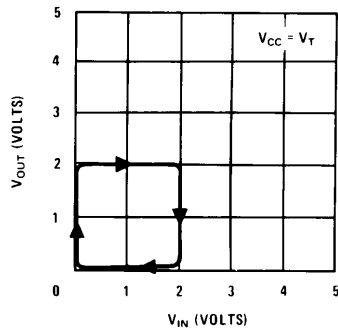
National also guarantees that its CMOS circuits have a 1V DC noise margin over the full power supply range and temperature range and with any combination of inputs. This is simply a variation of the noise immunity spec only now a specific set of input and output voltages have been selected and guaranteed. Stated verbally, the spec says that for the output of a circuit to be within $0.1 V_{CC}$ volts of a proper logic level (V_{CC} or Ground), the input can be as much as $0.1 V_{CC}$ plus 1V away from power supply rail. Shown graphically we have:



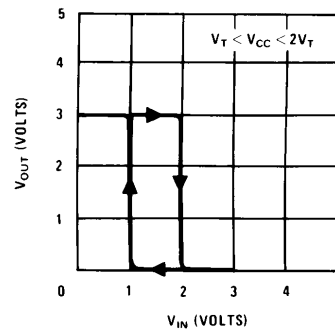
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FIGURE 2-5. Guaranteed CMOS DC margin over temperature as a function of V_{CC} . CMOS Guarantees 1V.

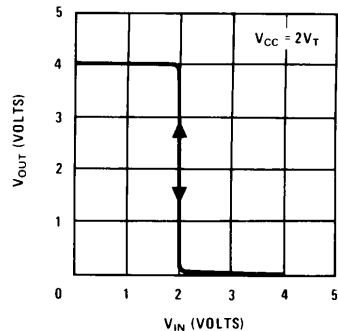
This is similar in nature to the standard TTL noise margin spec which is 0.4V.



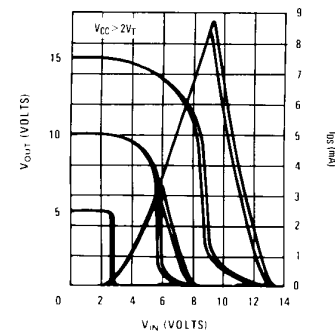
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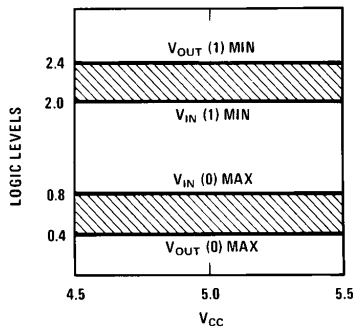


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FIGURE 2-4. Transfer Characteristics vs V_{CC}



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FIGURE 2-6. Guaranteed TTL DC margin over temperature as a function of V_{CC}. TTL Guarantees 1V.

For a complete picture of V_{OUT} vs V_{IN} refer to the transfer characteristic curves in Figure 2-4.

SYSTEM CONSIDERATIONS

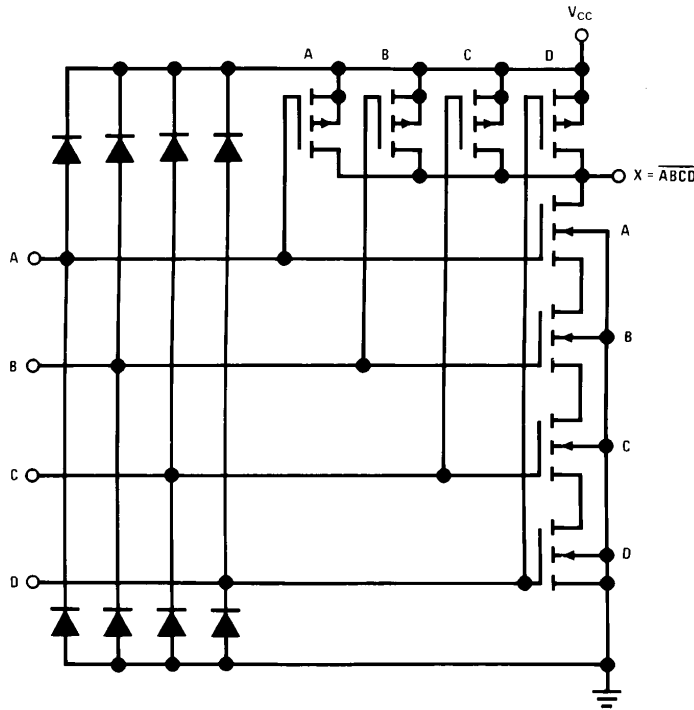
This section describes how to handle many of the situations that arise in normal system design such as unused inputs, paralleling circuits for extra drive, data bussing, power considerations and interfaces to other logic families.

Unused inputs: Simply stated, unused inputs should not be left open. Because of the very high impedance (~ 10¹²Ω), a

floating input may drift back and forth between a “0” and “1” creating some very intriguing system problems. All unused inputs should be tied to V_{CC}, Ground or another used input. The choice is not completely arbitrary, however, since there will be an effect on the output drive capability of the circuit in question. Take, for example, a four input NAND gate being used as a two input gate. The internal structure is shown in Figure 3-1. Let inputs A and B be the unused inputs.

If we are going to tie the unused inputs to a logic level, inputs A and B would have to be tied to V_{CC} to enable the other inputs to function. That would turn on the lower A and B transistors and turn off the upper A and B transistors. At most, only two of the upper transistors could ever be turned on. However, if inputs A and B were tied to input C, the input capacitance would triple, but each time C went low, the upper A, B and C transistors would turn on, tripling the available source current. If input D was low also, all four of the upper transistors would be on.

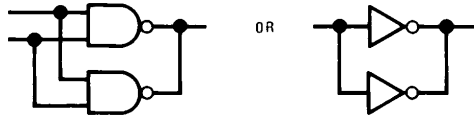
So, tying unused NAND gate inputs to V_{CC} (Ground for NOR gates) will enable them, but tying unused inputs to other used inputs guarantees an increase in source current in the case of NAND gates (sink current in the case of NOR gates). There is no increase in drive possible through the series transistors. By using this approach, a multiple input gate could be used to drive a heavy current load such as a lamp or a relay.



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FIGURE 3-1. MM74C20 Four Input NAND gate

Parallel gates: Depending on the type of gate, tying inputs together guarantees an increase in either source or sink current but not both. To guarantee an increase in both currents, a number of gates must be paralleled as in *Figure 3-2*. This insures that there are a number of parallel combinations of the series string of transistors (*Figure 3-1*), thereby increasing drive in that direction also.



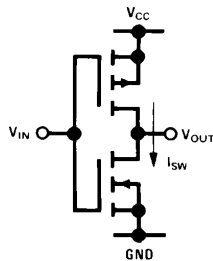
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FIGURE 3-2. Paralleling Gates or Inverters Increases Output Drive in Both Directions.

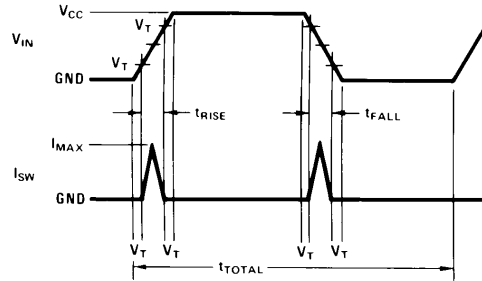
Data bussing: There are essentially two ways to do this. First, connect ordinary CMOS parts to a bus using transfer gates (Part No. CD4016C). Second, and the preferred way, is to use parts specifically designed with a CMOS equivalent of a TRI-STATE® output.

Power supply filtering: Since CMOS can operate over a large range of power supply voltages (3V to 15V), the filtering necessary is minimal. The minimum power supply voltage required will be determined by the maximum frequency of operation of the fastest element in the system (usually only a very small portion of any system operates at maximum frequency). The filtering should be designed to keep the power supply voltage somewhere between this minimum voltage and the maximum rated voltage the parts can tolerate. However, if power dissipation is to be kept to a minimum, the power supply voltage should be kept as low as possible while still meeting all speed requirements.

Minimizing system power dissipation: To minimize power consumption in a given system, it should be run at the minimum speed to do the job with the lowest possible power



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VI Power is Given By:

$$P_{VI} = V_{CC} \times \frac{1}{2} I_{MAX} \times \text{Rise Time to Period Ratio}$$

$$\text{Rise Time to Period Ratio} = \frac{V_{CC} - 2V_T}{V_{CC}} \times \frac{t_{RISE} + t_{FALL}}{t_{TOTAL}}$$

$$\text{Where } \frac{1}{t_{TOTAL}} = \text{Frequency}$$

$$P_{VI} = \frac{1}{2} (V_{CC} - 2V_T) I_{CC \text{ Max}} (t_{RISE} + t_{FALL}) \text{ FREQ.}$$

FIGURE 3-3. DC Transient Power

supply voltage. AC and DC transient power consumption both increase with frequency and power supply voltage. The AC power is described as CV^2f power. This is the power dissipated in a driver driving a capacitive load. Obviously, AC power consumption increases directly with frequency and as the square of the power supply. It also increases with capacitive load, but this is usually defined by the system and is not alterable. The DC power is the VI power dissipated during switching. In any CMOS device during switching, there is a momentary current path from the power supply to ground, (when $V_{CC} > 2V_T$) *Figure 3-3*.

The maximum amplitude of the current is a rapidly increasing function of the input voltage which in turn is a direct function of the power supply voltage. See *Figure 2-4d*.

The actual amount of VI power dissipated by the system is determined by three things: power supply voltage, frequency and input signal rise time. A very important factor is the input rise time. If the rise time is long, power dissipation increases since the current path is established for the entire period that the input signal is passing through the region between the threshold voltages of the upper and lower transistors. Theoretically, if the rise time were zero, no current path would be established and the VI power would be zero. However, with a finite rise time there is always some current flow and this current flow increases rapidly with power supply voltage.

Just a thought about rise time and power dissipation. If a circuit is used to drive many loads, its output rise time will suffer. This will result in an increase in VI power dissipation in every device being driven by that circuit (but not in the drive circuit itself). If power consumption is critical, it may be necessary to improve the rise time of that circuit by buffering or by dividing the loads in order to reduce overall power consumption.

So, to summarize the effects of power supply voltage, input voltage, input rise time and output load capacitance on system power dissipation, we can say the following:

1. **Power supply voltage:** CV^2f power dissipation increases as the square of power supply voltage. VI power dissipation increases approximately as the square of the power supply voltage.
2. **Input voltage level:** VI power dissipation increases if the input voltage lies somewhere between Ground plus a threshold voltage and V_{CC} minus a threshold voltage. The highest power dissipation occurs when V_{IN} is at $\frac{1}{2} V_{CC}$. CV^2f dissipation is unaffected.
3. **Input rise time:** VI power dissipation increases with longer rise times since the DC current path through the device is established for a longer period. The CV^2f power is unaffected by slow input rise times.
4. **Output load capacitance:** The CV^2f power dissipated in a circuit increases directly with load capacitance. VI power in a circuit is unaffected by its output load capacitance. However, increasing output load capacitance will slow down the output rise time of a circuit which in turn will affect the VI power dissipation in the devices it is driving.

INTERFACES TO OTHER LOGIC TYPES

There are two main ideas behind all of the following interfaces to CMOS. First, CMOS outputs should satisfy the current and voltage requirements of the other family's inputs. Second, and probably most important, the other family's outputs should swing as near as possible to the full voltage range of the CMOS power supplies.

P-Channel MOS: There are a number of things to watch for when interfacing CMOS and P-MOS. The first is the power supply set. Most of the more popular P-MOS parts are specified with 17V to 24V power supplies while the maximum power supply voltage for CMOS is 15V. Another problem is that unlike CMOS, the output swing of a push-pull P-MOS output is significantly less than the power supply voltage across it. P-MOS swings from very close to its more positive supply (V_{SS}) to quite a few volts above its more negative

supply (V_{DD}). So, even if P-MOS uses a 15V or lower power supply set, its output swing will not go low enough for a reliable interface to CMOS. There are a number of ways to solve this problem depending on the configuration of the system. We will discuss two solutions for systems that are built totally with MOS and one solution for systems that include bipolar logic.

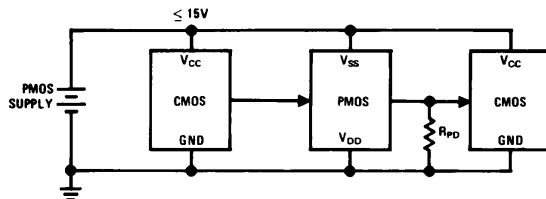
First, MOS only. P-MOS and CMOS using the same power supply of less than 15V, *Figure 3-4*.

In this configuration CMOS drives P-MOS directly. However, P-MOS cannot drive CMOS directly because of its output will not pull down close enough to the lower power supply rail. R_{PD} (R pull down) is added to each P-MOS output to pull it all the way down to the lower rail. Its value is selected such that it is small enough to give the desired RC time constant when pulling down but not so small that the P-MOS output cannot pull it virtually all the way up to the upper power supply rail when it needs to. This approach will work with push-pull as well as open drain P-MOS outputs.

Another approach in a purely MOS system is to build a cheap zener supply to bias up the lower power supply rail of CMOS, *Figure 3-5*.

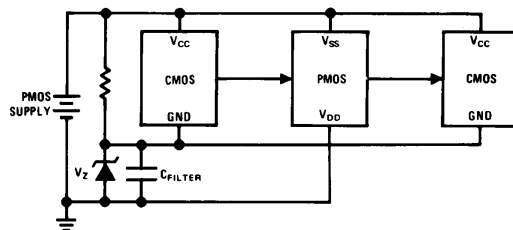
In this configuration the P-MOS supply is selected to satisfy the P-MOS voltage requirement. The bias supply voltage is selected to reduce the total voltage across the CMOS (and therefore its logic swing) to match the minimum swing of the P-MOS outputs. The CMOS can still drive P-MOS directly and now the P-MOS can drive CMOS with no pull-down resistors. The other restrictions are that the total voltage across the CMOS is less than 15V and that the bias supply can handle the current requirements of all the CMOS. This approach is useful if the P-MOS supply must be greater than 15V and the CMOS current requirement is low enough to be done easily with a small discrete component regulator.

If the system has bipolar logic, it will usually have at least two power supplies. In this case, the CMOS is run off the bipolar supply and it interfaces directly to P-MOS, *Figure 3-6*.



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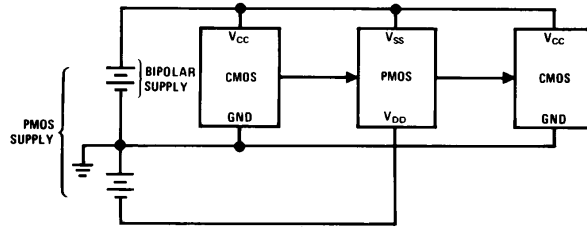
FIGURE 3-4. A One Power Supply System Built Entirely of CMOS and P-MOS



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Use a Bias supply to reduce the voltage across the CMOS to match the logic swing of the P-MOS. Make sure the resulting voltage across the CMOS is less than 15V.

FIGURE 3-5. A P-MOS and CMOS System Where the P-MOS Supply is Greater than 15V

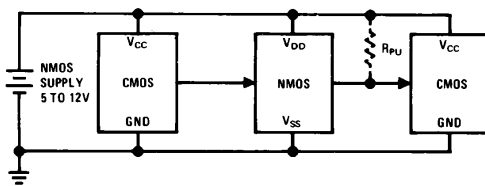


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Run the CMOS from the bipolar supply and interface directly to P-MOS.
FIGURE 3-6. A System with CMOS, P-MOS and Bipolar Logic

N-Channel MOS: Interfacing to N-MOS is somewhat simpler than interfacing to P-MOS although similar problems exist. First, N-MOS requires lower power supplies than P-MOS, being in the range of 5V to 12V. This is directly compatible with CMOS. Second, N-MOS logic levels range from slightly above the lower supply rail to about 1V to 2V below the upper rail.

At the higher power supply voltages, N-MOS and CMOS can be interfaced directly since the N-MOS high logic level will be only about 10 to 20 percent below the upper rail. However, at lower supply voltages the N-MOS output will be down 20 to 40 percent below the upper rail and something may have to be done to raise it. The simplest solution is to add pull up resistors on the N-MOS outputs as shown in Figure 3-7.



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Both operate off same supply with pull up resistors optional from N-MOS to CMOS.

FIGURE 3-7. A System with CMOS and N-MOS Only

TTL, LPTTL, DTL: Two questions arise when interfacing bipolar logic families to CMOS. First, is the bipolar family's logic "1" output voltage high enough to drive CMOS directly?

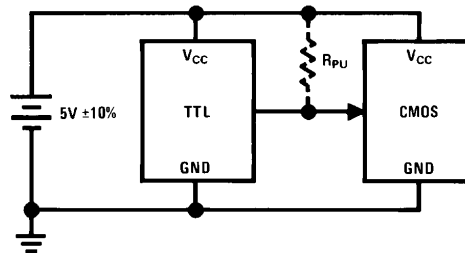
TTL, LPTTL, and DTL can drive 74C series CMOS directly over the commercial temperature range without external pull up resistors. However, TTL and LPTTL cannot drive 4000 series CMOS directly (DTL can) since 4000 series specs do not guarantee that a direct interface with no pull up resistors will operate properly.

DTL and LPTTL manufactured by National (NS LPTTL pulls up one diode drop higher than the LPTTL of other vendors) will also drive 74C directly over the entire military temperature range. LPTTL manufactured by other vendors and standard TTL will drive 74C directly over most of the military temperature range. However, the TTL logic "1" drops to a somewhat marginal level toward the lower end of the military temperature range and a pull up resistor is recommended.

According to the curve of DC margin vs V_{CC} for CMOS in Figure 2-5, if the CMOS sees an input voltage greater than $V_{CC} - 1.5V$ ($V_{CC} = 5V$), the output is guaranteed to be less than 0.5V from Ground. The next CMOS element will amplify this 0.5V level to the proper logic levels of V_{CC} or Ground. The standard TTL logic "1" spec is a V_{OUT} min. of 2.4V sourcing a current of 400 μA . This is an extremely conservative spec since a TTL output will only approach a one level of 2.4V under the extreme worst case conditions of lowest temperature, high input voltage (0.8V), highest possible leakage currents (into succeeding TTL devices), and V_{CC} at the lowest allowable ($V_{CC} = 4.5V$).

Under nominal conditions (25°C, $V_{IN} = 0.4V$, nominal leakage currents into CMOS and $V_{CC} = 5V$) a TTL logic "1" will be more like $V_{CC} - 2V_D$, or $V_{CC} - 1.2V$. Varying only temperature, the output will change by two times -2 mV per °C, or -4 mV per °C. $V_{CC} - 1.2V$ is more than enough to drive CMOS reliably without the use of a pull up resistor.

If the system is such that the TTL logic "1" output can drop below $V_{CC} - 1.5V$, use a pull up resistor to improve the logic "1" voltage into the CMOS.



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Pull up resistor, R_{PU} , is needed only at the lower end of the Mil temperature range.

FIGURE 3-8. TTL to CMOS Interface

The second question is, can CMOS sink the bipolar input current and not exceed the maximum value of the bipolar logic zero input voltage? The logic "1" input is no problem.

The LPTTL input current is small enough to allow CMOS to drive two loads directly. Normal power TTL input currents are ten times higher than those in LPTTL and consequently the CMOS output voltage will be well above the input logic "0" maximum of 0.8V. However, by carefully examining the CMOS output specs we will find that a two input NOR gate can drive one TTL load, albeit somewhat marginally. For example, the logical "0" output voltage for both an MM74C00 and MM74C02 over temperature is specified at 0.4V sinking 360 μA (about 420 μA at 25°C) with an input voltage of 4.0V and a V_{CC} of 4.75V. Both schematics are shown in Figure 3-9.

Both parts have the same current sinking spec but their structures are different. What this means is that either of the lower transistors in the MM74C02 can sink the same current as the two lower series transistors in the MM74C00. Both MM74C02 transistors together can sink twice the specified current for a given output voltage. If we allow the output voltage to go to 0.8V, then a MM74C02 can sink four times 360 μ A, or 1.44 mA which is nearly 1.6 mA. Actually, 1.6 mA is the maximum spec for the TTL input current and most TTL parts run at about 1 mA. Also, 360 μ A is the minimum CMOS sink current spec, the parts will really sink somewhere between 360 μ A and 540 μ A (between 2 and 3 LPTTL input loads). The 360 μ A sink current is specified with an input voltage of 4.0V. With an input voltage of 5.0V, the sink current will be about 560 μ A over temperature, making it even easier to drive TTL. At room temperature with an input voltage of 5V, a CMOS output can sink about

800 μ A. A 2 input NOR gate, therefore, will sink about 1.6 mA with a V_{OUT} of about 0.4V if both NOR gate inputs are at 5V.

The main point of this discussion is that a common 2 input CMOS NOR gate such as an MM74C02 can be used to drive a normal TTL load in lieu of a special buffer. However, the designer must be willing to sacrifice some noise immunity over temperature to do so.

TIMING CONSIDERATIONS IN CMOS MSIs

There is one more thing to be said in closing. All the flip-flops used in CMOS designs are genuinely edge sensitive. This means that the J-K flip-flops do not "ones catch" and that some of the timing restrictions that applied to the control lines on MSI functions in TTL have been relaxed in the 74C series.

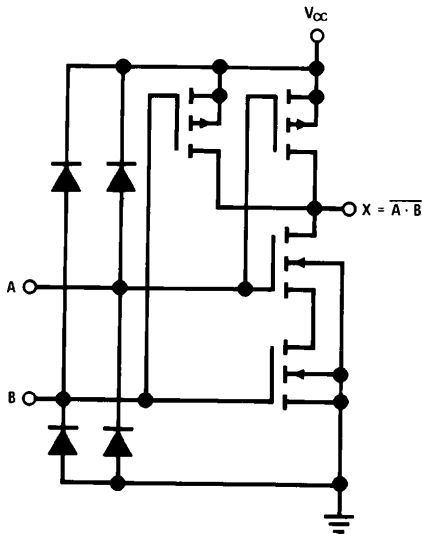


FIGURE 3-9a. MM74C00

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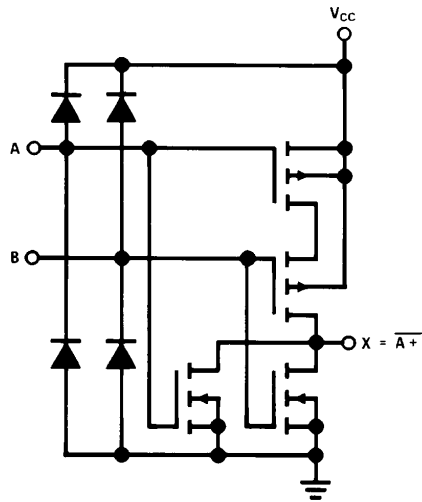


FIGURE 3-9b. MM74C02

TL/F/6019-21

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National Semiconductor Corporation
 1111 West Bardin Road
 Arlington, TX 76017
 Tel: (800) 272-9959
 Fax: (800) 737-7018

National Semiconductor Europe
 Fax: (+49) 0-180-530 85 86
 Email: cnjwge@tevm2.nsc.com
 Deutsch Tel: (+49) 0-180-530 85 85
 English Tel: (+49) 0-180-532 78 32
 Français Tel: (+49) 0-180-532 93 58
 Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
 19th Floor, Straight Block,
 Ocean Centre, 5 Canton Rd.
 Tsimshatsui, Kowloon
 Hong Kong
 Tel: (852) 2737-1600
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